University of Alberta

VOLTAGE REFERENCES USING MUTUAL COMPENSATION OF MOBILITY AND THRESHOLD VOLTAGE TEMPERATURE EFFECTS

by

Laleh Najafizadeh

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Abstract

A voltage reference is an essential building block of many analog and digital circuits. The performance of a reference is gauged by the maximum variation in its allowable operating conditions. One of the most important specifications of a reference is its temperature drift. Therefore, special attention should be paid by the designer to the thermal behavior of a voltage reference.

In this thesis, three new voltage reference circuits are proposed and designed in 0.18-μm technology. Our goal has been to design CMOS voltage references with better temperature stability compared to that of existing voltage references. First, a voltage reference is presented which takes advantage of summing the gate-source voltages of two diode-connected transistors biased by temperature-stable currents. The temperature coefficient of the output voltage of this reference is shown to be 28 ppm/°C over the temperature range of -50°C to 150°C. Next, the temperature behavior of the gate-source voltage of a CMOS transistor biased by a current, which is proportional to absolute temperature (PTAT), is investigated. It is shown that the temperature coefficient of the gate-source voltage of the transistor can be altered by adjusting the parameters of the PTAT current source. This idea is then applied to the design of two temperature-independent voltage references. The first reference consists of a PTAT current source and a diode-connected transistor. Simulation results show that the temperature coefficient of this reference voltage is 4 ppm/°C over the range

of -50°C to 150°C. The second reference takes advantage of summing the gate-source voltages of two NMOS transistors biased by PTAT currents. The last two references show a temperature coefficient of 4 ppm/°C over the range of -50°C to 150°C and can operate with a power supply below 1 V. The simulation results for this voltage reference show a temperature coefficient of 4 ppm/°C over the range of -50°C to 150°C. The operation of all the circuits are also justified analytically.

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Acronyms

A/D	analog to digital
BGR	bandgap reference
BJT	bipolar junction transistor
CM	current mode
CTAT	complementary to absolute temperature
CMOS	complementary metal oxide semiconductor
D/A	digital to analog
DRAM	dynamic random access memory
DTMOS	dynamic threshold metal oxide semiconductor transistors
FET	field effect transistor
MOS	metal oxide semiconductor
PLL	phase locked loop
PTAT	proportional to absolute temperature
TC	temperature coefficient
TI	temperature independent
ZTC	zero temperature coefficient

List of Symbols

C_{ox}	Gate oxide capacitor
E_g	Energy bandgap
E_{g0}	Extrapolated zero-degree bandgap energy
I_B	The bias current
I_C	The collector current
I_D	The drain current
I_s	The saturation current
J_s	Saturation current density
k	Boltzmann constant
kT	Thermal energy
L	Length of a MOS transistor gate
m	Mobility parameter
m_0	Free electron mass
m_{de}	Electron effective mass
m_{dh}	Hole effective mass
n_c	Carrier concentration
n_i	Intrinsic carrier concentration
N_A	Acceptor concentration
N_D	Donor concentration

N_I	Impurity concentration
N_p	Carrier concentration in the polysilicon gate
N_s	Substrate doping
q	Electron charge
Q_i	The implanted charge per unit area
Q_{ss}	The surface-state charge density per unit area
R_B	The bias resistor
T	Absolute temperature
t_{ox}	Gate-oxide thickness
T_0	Correction term owing to the threshold shift implant
V_0	
V_{BE}	The base-emitter voltage
V_{DD}	The power supply voltage
$V_{DD_{\min}}$	Minimum required power supply
V_{DS}	The drain-source voltage
$V_{DS_{sat}}$	The saturated drain-source voltage
V_{G0}	The bandgap voltage of silicon extrapolated to 0°K
V_{GS}	The gate-source voltage
V_{ref}	The reference voltage
V_{SB}	The source-body voltage
V_T	Thermal voltage
V_{TH}	Threshold voltage
V_{THp}	PMOS threshold voltage
V_{THn}	NMOS threshold voltage
W	Width of a MOS transistor gate

α_{R1}	First order temperature coefficient of a resistor
α_{R2}	Second order temperature coefficient of a resistor
α_{VT}	Temperature coefficient of Threshold Voltage
μ	Carrier mobility
μ_e	Electron mobility
μ_h	Hole mobility
μ_I	Carrier mobility impeded by impurity scattering
μ_L	Carrier mobility impeded by lattice scattering
ϕ_{b1}	Barrier lowering voltage
ϕ_F	Fermi level
ϕ_{ms}	Metal-semiconductor work function differnece

Chapter 1

Introduction

1.1 Motivation

Most, if not all, electrical circuits use a reference, be it voltage, current or time. A reference in a circuit establishes a stable point used by other sub-circuits to generated predictable and repeatable results. This reference point should not change significantly under various operating conditions. Temperature is an important parameter which affects the performance of references. Special attention should therefore be paid by the designer to the temperature behavior of the reference. The typical metric used for variations of the reference voltage across temperature is the temperature coefficient (TC) and it is normally expressed in parts-per-million per degree Celsius (ppm/°C),

$$\mathrm{TC_{ref}} = \frac{1}{\mathrm{Reference}} \frac{\partial \mathrm{Reference}}{\partial \mathrm{Temperature}}, \tag{1.1}$$

where the reference is either in volts, amps, or seconds [1].

Current references are used in most of the basic building blocks. Usually, the current in different basic blocks results from mirroring of one or more references. Therefore, it is important that the master current of the system to be power-supply

independent and designed with the required accuracy. Current references are also used for the design of voltage references. A current reference typically does not need to be temperature-independent, however, its temperature coefficient should be well characterized and controlled.

Voltage references have been used in various fields of application, for example in digital to analog (D/A) converters, the automotive industry and in battery-operated DRAMs [2]. In D/A converters, depending on the digital input word, the analog voltage is a fraction of the internal reference voltage. As for many applications this digital to analog conversion should not depend on temperature, so the reference voltage has to be temperature-independent. Nowadays, high resolution D/A converters are being used and consequently the reference voltage must be very stable as each variation in the reference voltage is directly sensed in the D/A-converter output.

In the automotive industry electronic circuits are used to realize larger systems with more functions. However, the automotive environment, is very extreme and the temperature variations can be in the range of -15°C to 105°C. A supply voltage regulator handles the stabilization of the supply voltage in the car and the reference for this regulator must be able to withstand the extreme automotive environment [2]. Similarly, in battery-operated DRAMs, voltage references are used for power-supply voltage stabilization. In this case, the power consumption is of prime importance.

Bandgap voltage references are the most popular precise references used in various circuits. A bandgap voltage reference (BGR) has high power rejection and its output voltage is very stable against temperature and process variations. It can be implemented using available, vertical or lateral BJTs in any standard CMOS technology [3],[4]. However, when the supply voltage falls below 1 V, the performance of a conventional bandgap reference degrades [5]. As an alternative, voltage references

can also be implemented in MOS technology using the threshold voltage difference [6]. But this solution requires multi-threshold transistors which are not applicable in standard low-cost CMOS technologies since additional fabrication steps are needed. The development of other techniques for the design of low-voltage CMOS voltage references is therefore needed, a CMOS voltage reference whose performance is comparable to the performance of bandgap references.

1.2 Thesis Outline and Contribution

To successfully design a CMOS current/voltage reference, one must have a thorough understanding of the temperature behavior of MOS transistors. Therefore, in Chapter 2, we briefly describe the temperature dependency of some basic semiconductor physical properties (energy bandgap, intrinsic carrier concentration, impurity carrier concentration and Fermi potential) and the effects of temperature on MOS transistor parameters (threshold voltage and carrier mobility). The equations which are generally used to describe the temperature behavior of the CMOS threshold voltage and mobility are presented. The presence of the zero temperature coefficient (ZTC) point in the transconductance characteristics of a CMOS transistor is studied and the conditions under which such a point can exist are investigated.

In Chapter 3, we will study the techniques used for the design of different types of current references. Generally, current references based on their temperature performances are categorized into 4 groups. A proportional-to-absolute temperature current reference, as the name implies, generates a current which is linearly proportional to temperature. In a complementary-to-absolute temperature (CTAT) reference, the complement of a PTAT reference, generates a current which decreases as the

temperature increases. Temperature-independent current references are another category, and are usually designed based on properly combining temperature-dependent currents or using available voltage references. The last group of current references generate a square PTAT current ($PTAT^2$) which is proportional to the square of the temperature. The design methods and the operation basics of these current references are studied in this chapter.

In Chapter 4 we will review the theory and the issues, with respect to temperature, that surround the design of different groups of voltage references. We begin by reviewing the techniques used for the design of most widely used voltage references in electronics circuit, i.e., the bandgap references. To get a clear insight, the basic function of bandgap references is studied first, including a general description of the temperature compensation. Then, as the basic structure is found, the techniques used for the design of first-order bandgap references will be studied. Thereafter, some special structures, such as quadratic temperature compensation, second-order curvature-compensated reference using resistor ratios and piecewise-linear curvature correction to improve the temperature behavior of bandgap references will be given. Also, the methods used for the design of low-voltage BGR are studied. Finally, we present techniques used for the implementation of CMOS non-bandgap voltage references (such as references based on threshold-voltage difference, weighted gate-source voltage difference and ZTC point) which have performance comparable to the performance of BGR.

In Chapter 5, it is shown that the temperature dependency of the gate-source voltage of a CMOS transistor biased with a PTAT current source can be altered by adjusting the parameters of the PTAT current source. A circuit consisting of a diode-connected transistor biased by a PTAT current source is designed and implemented

in 0.18-μm CMOS technology. The parameters of the current source have been chosen in order to obtain a temperature-independent gate-source voltage. The circuit is simulated successfully and the simulation results are also given. A sub-1-V CMOS voltage reference, which takes advantage of summing the gate-source voltages of two NMOS transistors operating in the saturation region, is also presented. Both transistors are working below the zero temperature coefficient point and, thus, the voltage reference is able to operate with a low supply voltage. This circuit is implemented in a standard 0.18-μm CMOS process and the simulation results are given. To the best of the author's knowledge, this is a new approach for the design of CMOS voltage references. The performances of the proposed voltage references are compared with other voltage references in the literature and it is shown that our voltage references have a comparable performance with the bandgap voltage references and a better performance than the non-bandgap ones.

Finally, the conclusions and a summary of the thesis are given in Chapter 6.

Chapter 2

The Basics

In this chapter, we consider some basic properties of semiconductor materials with emphasis on the temperature dependencies of these properties. This is followed by the discussion of the temperature dependency of the threshold voltage and the carrier mobility in a MOS transistor. Then the zero temperature coefficient (ZTC) point in CMOS transistors will be presented and the conditions under which this point exists are investigated.

2.1 Basic Semiconductor Effects

In this section, we review the temperature dependencies of some basic properties of semiconductor materials.

Energy Bandgap: The difference in energy between the valence band and the conduction band is called the energy bandgap and is denoted by E_g. The temperature dependency of E_g of silicon is given by [7]

$$E_g(T) = 1.170 - \frac{4.73 \times 10^{-4} T^2}{T + 636}. \tag{2.1}$$

where T is the absolute temperature in K. Figure 2.1 shows the temperature de-

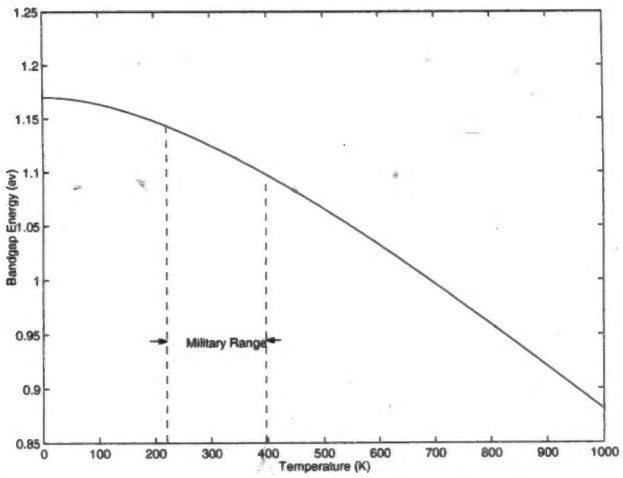


Figure 2.1: Silicon bandgap energy as a function of temperature

pendency of the silicon bandgap energy. As it can be seen, even for the relatively broad military temperature range of $-55°C$ to $125°C$ ($218°K$-$398°K$), E_g has a weak temperature dependence.

Intrinsic Carrier Concentration: The concentration n_i of intrinsic electrons and holes depends on the amount of energy needed to break a bond (e.g., the energy bandgap) and on the amount of energy available (e.g., the thermal energy as characterized by the temperature) [8]. The mathematical relationship between these parameters is given by [9]

$$n_i = 4.9 \times 10^{15} \left(\frac{m_{de} m_{dh}}{m_0^2} \right)^{3/4} T^{3/2} exp\left(\frac{-E_g}{2kT} \right) = AT^{3/2} exp\left(\frac{-E_g}{2kT} \right) \qquad (2.2)$$

where k is the Boltzmann's constant, m_{de} and m_{dh} are the electron and hole effective masses and m_0 is the free electron mass.

Carrier Concentration: When impurity atoms are added and at relatively elevated temperature, when most donors and acceptors are ionized, carrier concentration, n_c, can be expressed by [10]

$$n_c = \begin{cases} \frac{1}{2}\left[(N_D - N_A) + \sqrt{(N_D - N_A)^2 + 4n_i^2}\right] & (n\text{-type}) \\ \\ \frac{1}{2}\left[(N_A - N_D) + \sqrt{(N_D - N_A)^2 + 4n_i^2}\right] & (p\text{-type}) \end{cases} \tag{2.3}$$

where N_D and N_A are donor and acceptor concentration, respectively. As long as the magnitude of the net impurity concentration $|N_D - N_A|$ is much larger than n_i, the intrinsic carrier concentration, will be approximately equal to the substrate doping concentration (i.e.,$(N_D - N_A)$ for n-type and $(N_A - N_D)$ for p-type).

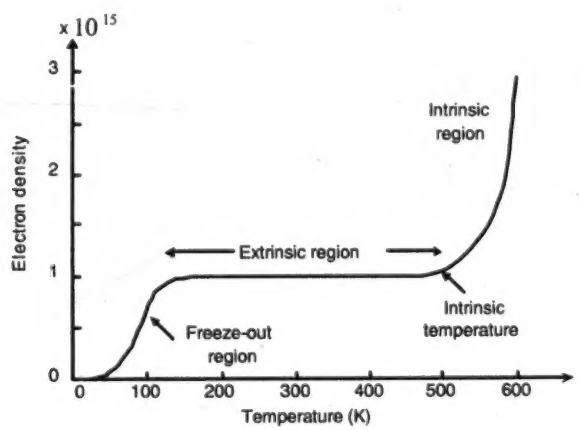


Figure 2.2: Electron density as a function of temperature for a Si sample with a donor concentration of $N_D = 10^{15} cm^{-3}$ (after [10])

Figure 2.2 shows the carrier concentration in Si as a function of temperature for a donor concentration of $N_D = 10^{15} cm^{-3}$. When the temperature is low, the thermal energy is not sufficient to ionize all the impurities and so the carrier density is less than the donor concentration. This region is known as freeze-out region. As

the temperature increases, all impurities are ionized and $n_c = N_D$. This condition will remain over a wide temperature range and is known as extrinsic region. However, as the temperature is increased further, the intrinsic carrier concentration, n_i, is increased as well and we reach a point where the intrinsic carrier concentration becomes comparable to N_D. The temperature at which the intrinsic carrier concentration becomes equal to N_D, is called the intrinsic temperature. It is apparent that the intrinsic temperature can be delayed by increasing the impurity density.

Fermi Level: For an intrinsic semiconductor, the Fermi level lies about midway between the valence and conduction bands. The Fermi level in n-type materials is closer to the conduction band while for p-type material it is closer to the valence band. The value of the Fermi level depends on temperature due to the temperature dependence of n_i and the thermal voltage, $V_T = \frac{kT}{q}$, and is expressed by

$$\phi_F(T) = \pm\frac{kT}{q}\ln\left(\frac{n_c}{n_i(T)}\right) \tag{2.4}$$

where the positive or negative sign refers to n-type or p-type semiconductors, respectively.

2.2 Threshold Voltage

A commonly used expression for the threshold voltage of the MOS transistor is given by [11]

$$V_{TH} = \phi_{ms} \pm \frac{Q_{ss}}{C_{ox}} + 2\phi_F + \Delta V_T(N_i) \pm \gamma(N_s, t_{ox}, L, W)\sqrt{2\phi_F + V_0 + |V_{SB}|} \tag{2.5}$$

where the positive or negative sign refers to n-channel or p-channel devices, respectively. In this equation: ϕ_{ms} is the metal-silicon work function difference, Q_{ss} is the surface-state charge density per unit area, C_{ox} is the gate-oxide capacitance per unit

area, ϕ_F is the Fermi potential of the substrate, $\Delta V_T(N_i)$ is the threshold shift owing to a channel implant N_i with depth, d_i, and γ is the body-effect constant that depends on the substrate doping N_s, the gate-oxide thickness t_{ox}, the channel length L and width W. Finally, $V_0(N_i, N_s, d_i)$ is a correction term owing to the threshold shift implant. For enhancement devices with a ΔV_T shifting implant of the same type as the substrate, V_0 has a sign opposite to that of ϕ_F.

The major contributions to the variation of threshold voltage with temperature are the Fermi level, ϕ_F, and the gate-semiconductor work function difference, ϕ_{ms}. The Fermi level is expressed by equation (2.4). For a silicon gate doped oppositely to the substrate, the contact potential is essentially determined by the pn product. Therefore, for an n-type doped gate, the gate-semiconductor work function is expressed as [12]

$$\phi_{ms}(T) = \begin{cases} -\dfrac{kT}{q}\ln\left(\dfrac{N_s N_p}{n_i^2}\right) & (NMOS) \\ \\ -\dfrac{kT}{q}\ln\left(\dfrac{N_s}{N_p}\right) & (PMOS) \end{cases} \tag{2.6}$$

where N_p is the carrier concentration in the polysilicon gate. The temperature-dependent terms in Equation (2.6) are the intrinsic carrier concentration, n_i, and the thermal voltage, $\dfrac{kT}{q}$. The influence of the work function on the temperature behavior of the threshold voltage is often neglected in the literature [9]. But it has been shown that assuming a temperature-independent ϕ_{ms} affects the accuracy in predicting the threshold voltage temperature behavior, especially at temperatures above 373°K.

The minor contributions to the variation of threshold voltage with temperature are the variation in oxide capacitance, as well as the ionization of surface states [7]. To a first-order approximation these effects are very small and can be safely ignored.

It has been shown in [13] that the threshold voltage decreases approximately

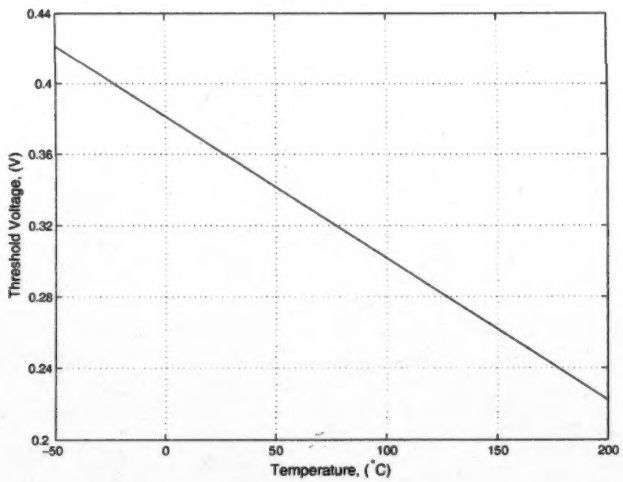


Figure 2.3: Threshold voltage of an NMOS transistor (W/L=2/1) as a function of temperature

linearly with an increase in temperature. Equation (2.7), given below, is usually used to show the temperature dependency of threshold voltage

$$V_{TH}(T) = V_{TH}(T_0) - \alpha_{VT}(T - T_0). \tag{2.7}$$

Figure 2.3 shows that the threshold voltage is a linear function of temperature. To generate Figure 2.3 a NMOS transistor, operating in saturation, is simulated and the plot of $\sqrt{I_D} = \sqrt{K(T)}(V_{GS} - V_{TH})$ versus V_{GS} is obtained for different temperatures, where I_D is the drain current, V_{GS} is the gate-source voltage and $K(T)$ depends on the transistor parameters. Then, using extrapolation of the simulated data, the value of the threshold voltage, V_{TH}, is obtained for different temperatures and is plotted as a function of temperature in Figure 2.3.

As the plot shows the temperature dependency of the threshold voltage can be closely approximated as a linear function of temperature. The temperature coefficient of the threshold voltage (TCVT), α_{VT}, is generally calculated by differentiating

equation (2.5) with respect to the temperature. Considering the fact that ϕ_F and ϕ_{ms} are the major factors which may cause a temperature dependence in the threshold voltage, α_{VT} will be equal to

$$\alpha_{VT} = |\frac{\partial V_{TH}}{\partial T}| = |\frac{\partial \phi_{ms}}{\partial T} + 2\frac{\partial \phi_F}{\partial T} + \frac{\gamma}{\sqrt{2\phi_F + V_0 + |V_{SB}|}}\frac{\partial \phi_F}{\partial T}|. \tag{2.8}$$

Assuming (2.2), where $\frac{E_{G0}}{q} = 1.21V$ is the extrapolated zero-degree band gap [14], and using (2.6), one can find that for an n-type doped gate

$$\frac{\partial \phi_{ms}}{\partial T} = \frac{1}{T}\left[\phi_{ms} + \frac{E_{G0}}{q} + \frac{3kT}{q}\right]. \tag{2.9}$$

Using (2.4), the temperature coefficient of ϕ_F is given by

$$\frac{\partial \phi_F}{\partial T} = \frac{1}{T}\left[\phi_F - \left(\frac{E_{G0}}{2q} + \frac{3kT}{2q}\right)\right]. \tag{2.10}$$

Therefore, the temperature coefficient of the threshold voltage becomes

$$\alpha_{VT} = |\frac{\partial V_{TH}}{\partial T}| = |\frac{\phi_{ms}}{T} + 2\frac{\phi_F}{T} + \frac{\gamma(N_s, t_{ox}, L, W)}{\sqrt{2\phi_F + V_0 + |V_{SB}|}}| \tag{2.11}$$

The value of α_{VT} varies [13], [15] from 1 mV/°C to 4 mV/°C. A most frequently used figure is 2 mV/°C [14]. Although the value of α_{VT} is assumed to be constant, there are a number of factors which affect its value. As equation (2.11) shows, the value of the temperature coefficient of threshold voltage depends on the value of $|V_{SB}|$. Higher back biases leads to a smaller value of TCVT. The length of the transistor also affects the value of the threshold voltage temperature coefficient. For a short channel transistor, the magnitude of TCVT is smaller due to the fact that part of the depletion charge associated with channel formation is depleted from the source and drain rather than from the gate. This effect leads to a reduction of the body effect, γ, resulting in the decrease of the temperature coefficient of the threshold voltage [11]. The dependency of TCVT on the length of transistor, is shown in Figure 2.4. As it

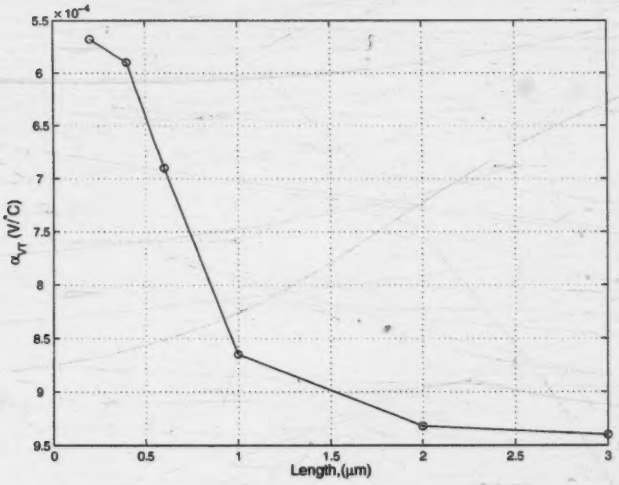


Figure 2.4: Change of α_{VT} with the length of an NMOS transistor with W=5

can be seen, only for the channel lengths greater than 2μm can α_{VT} be considered as a constant value.

2.3 Carrier Mobility

For nonpolar semiconductors, such as Si and Ge, the carrier mobility is affected by two basic scattering mechanisms: lattice scattering and impurity scattering [8], [10]. Lattice scattering results from thermal vibrations of the lattice atoms at any temperature above absolute zero. The interaction between the carriers and the lattice allow some energy to be transferred, leading to scattering. The mobility of carriers impeded by lattice scattering, μ_L, is given by [10]

$$\mu_L \sim (m^*)^{(-5/2)} T^{(-3/2)} \tag{2.12}$$

where m^* is the conductivity effect mass.

Impurity scattering is caused by distortion in the lattice, due to impurities such

as dopants. The mobility of carriers impeded by impurity scattering can be described by [10]

$$\mu_I \sim (m^*)^{-1/2} N_I^{-1} T^{3/2} \tag{2.13}$$

where N_I is the concentration of impurities. Equation (2.13) shows that as the impurity concentration increases, the mobility decreases. Also, as predicted by both equations (2.12) and (2.13), the mobility decreases as m^* increases. Therefore, for a given impurity concentration, the electron mobility is larger than the hole mobility.

At low temperatures, the carriers have low kinetic energy and their time of passage past ionized impurities is longer than at high temperature. Therefore, at low temperatures, impurity scattering dominates. As the temperature is increased, the carriers move faster, they remain near the impurity atom for a shorter time and therefore the collisions due to impurity scattering become less significant than the collisions with the neutral atoms of lattice. Thus, at high temperature, lattice scattering is the major scattering process and the carrier mobility will be proportional to $T^{-\frac{3}{2}}$. The combined mobility, which includes the two mechanisms above, is given by [8]

$$\frac{1}{\mu} = \left(\frac{1}{\mu_L} + \frac{1}{\mu_I} \right). \tag{2.14}$$

In the analysis of semiconductor devices it is often necessary to know the magnitude of the mobility for different doping densities and temperatures. Although this information is available from experimental figures [10], it is more convenient to have the data embodied in an equation which gives a good fit to the experimental data. Figure 2.5 shows the simulations of such equation (eq. (2.15)) presented in [8] for 3 different impurity concentrations.

$$\mu_e = 88(\frac{T}{300})^{-0.57} + \frac{7.4 \times 10^8 \times T^{-2.33}}{1 + [N/(1.26 \times 10^{17} \times (T/300)^{2.3})]0.88 \times (T/300)^{-0.146}} \tag{2.15}$$

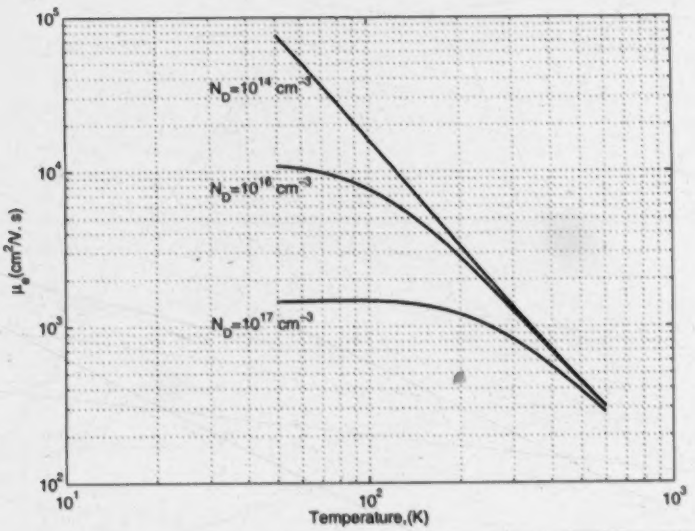


Figure 2.5: Mobility as a function of temperature

$$\mu_h = 54.3(\frac{T}{300})^{-0.57} + \frac{1.36 \times 10^8 \times T^{-2.23}}{1 + [N/(2.35 \times 10^{17} \times (T/300)^{2.4})]0.88 \times (T/300)^{-0.146}} \quad (2.16)$$

The curves in Figure 2.5 are a good fit to the experimental results given in [10]. As it can be seen, for lightly doped samples (e.g., the sample with doping of 10^{14}), lattice scattering dominates and the mobility decreases with temperature as is predicted by equation (2.12). However, the measured slope is different from $(-\frac{3}{2})$ because of the presence of other scattering mechanisms. The effect of impurity scattering becomes more significant at low temperatures for heavily doped samples and the mobility increases as the temperature increases. It can also be seen that, for a given temperature, the mobility decreases as the impurity concentration increases because of enhanced impurity scattering. This investigation shows that the slopes of the plots of mobility versus temperature could be different from $-\frac{3}{2}$, the number which is given in equation (2.12). A more general expression which is used to describe the

temperature dependency of the mobility is given by

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \tag{2.17}$$

where $\mu(T_0)$ is the mobility at the reference temperature, T_0, and $1 \leq m \leq 2.5$.

2.4 Zero Temperature Coefficient Point

The drain current of an NMOS transistor in the saturation region is given by [16]

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2. \tag{2.18}$$

In equation(2.18) the threshold voltage and the mobility are the main temperature-dependent parameters. As it was discussed earlier, as the temperature increases, both the threshold voltage and the mobility decrease. But the decrease of V_{TH} and the decrease of μ_n have opposing effects on the drain current; a lower threshold voltage tends to increase the drain current, but a lower mobility tends to decrease it. At some value of V_{GS}, this mutual compensation of mobility and threshold voltage results in a zero temperature coefficient, (ZTC), at a particular bias point of a MOS transistor. Figure 2.6 shows the simulated transconductance characteristics, with temperature as a parameter, for a NMOS transistor in 0.18μm CMOS technology. It can be seen that the transconductance characteristics have a common intercept point, which is clearly shown in the figure.

The conditions under which this compensation occurs and the stability of the ZTC point were investigated in detail in [14]. The gate-source voltage for which the drain current becomes temperature independent, at $T = T_1$, is obtained by setting the derivative of equation (2.18) with respect to the temperature, to zero, i.e.,

$$\frac{\partial I_D}{\partial T}|_{T=T1} = 0 \tag{2.19}$$

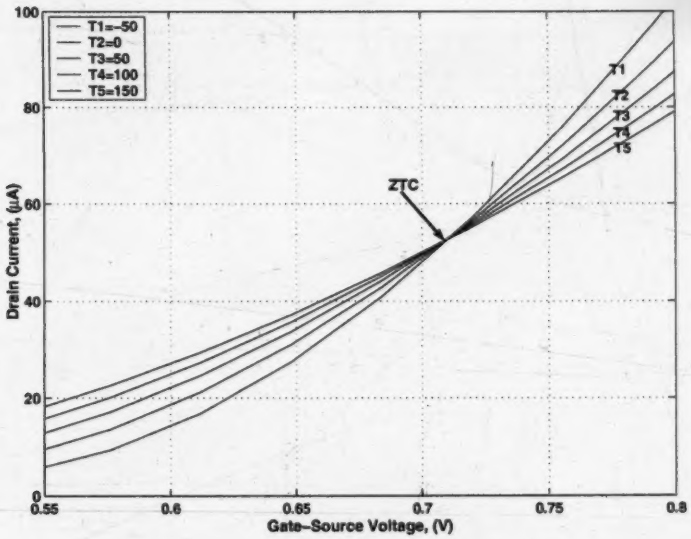


Figure 2.6: Transconductance characteristic for an NMOS transistor

which results in

$$V_{GS} = V_{TH}(T_1) + \left[2\mu_n \frac{\partial V_{TH}/\partial T}{\partial \mu_n/\partial T}\right]|_{T=T_1}. \tag{2.20}$$

By substituting equations (2.7) and (2.17) into (2.20), the desired gate-source voltage is obtained

$$V_{GS} = V_{TH}(T_0) - \alpha_{VT}T_1\left(1 - \frac{2}{m}\right) + \alpha_{VT}T_0. \tag{2.21}$$

A temperature-independent voltage will exist if $m = 2$. This voltage is equal to [14]

$$V_{GS} = V_{GSF} = V_{TH}(T_0) - \alpha_{VT}T_0 \tag{2.22}$$

and the drain current related to this bias voltage is equal to [14]

$$I_D = I_{DF} = \frac{\mu_n(T_0)T_0^2 C_{ox}}{2}\left(\frac{W}{L}\right)\alpha_{VT}^2. \tag{2.23}$$

Therefore, as reported in [14], when $m = 2$, the transconductance characteristics obtained at different temperatures have a common intercept point, known as the ZTC point, with parameters (V_{GSF}, I_{DF}). As it was mentioned in the previous section, the

value of m depends on the doping concentration and can become equal to 2. In the forthcoming chapters, we show that the ZTC point can be used for the design of temperature-independent voltage references.

2.5 Conclusion

In this chapter, some basic properties of semiconductor materials and their temperature dependencies were discussed. The threshold voltage and the mobility of a MOS transistor and their temperature behavior were studied. These two parameters are the major temperature-dependent parameters which affect the temperature behavior of a MOS transistor. It was shown that the mutual compensation of mobility and threshold voltage may result in the ZTC bias point of a MOS transistor. Also, the conditions under which a ZTC point exists were investigated.

Chapter 3

Current References

Current references are essential part of most analog and digital circuits. Amplifiers, phase-locked loops (PLLs) and oscillators are a few examples of the circuit applications of current references. These circuits are the fundamental building blocks of cellular phones, pagers, laptops and many other consumer electronic products.

The processing of current signals is done faster than the processing of voltage signals and, therefore, for a given technology, the circuits designed using current-mode approach operate faster than their voltage-mode counterparts. Moreover, the current value controls the transconductance of transistors and, in turn, affect the static and dynamic characteristics of circuits. Also, the performance of current sources influences the power consumption, which is an important parameter in many applications.

Often the current in different parts of a circuit results from the mirroring of one or more references. It is therefore important to study different techniques used for the design of current references and to recognize their functional limitations and to estimate the costs and benefits of each technique for the best design choice.

There are 4 types of current references which are commonly used in circuit designs. One type of current references generates a proportional-to-absolute temperature (PTAT) current, a current which is linearly proportional to temperature. Since the PTAT relation is predictable, and linear over a wide range of currents, this kind of current reference is the most frequently used reference. A complementary-to-absolute temperature (CTAT) current is also used as a reference current. A CTAT, the complement of PTAT, is often used in conjunction with curvature correction schemes for the design of precise voltage references [1], [17], [18], [19], [4]. Temperature-independent current references are usually designed based on properly combining temperature-dependent currents or using available voltage references. Square PTAT current ($PTAT^2$) references are another useful type of current references. The generated currents by these references are proportional to the square of the temperature. As we will see in the next chapter, this quadratic dependence to the temperature can be used to construct second-order voltage references.

In this chapter the techniques used for the design of these types of current references are studied and the benefits and disadvantages of each technique are discussed.

3.1 PTAT Current References

As the name implies, a PTAT current reference generates a current which increases as the temperature increases. Generally, these type of current references are obtained by forcing a PTAT built-in voltage across a resistor.

The difference of the base-emitter voltage of two bipolar transistors is proportional to the temperature and can be used for the design of PTAT current references.

The relationship between the base-emitter voltage of an *npn* transistor and its

collector current is expressed by [1]

$$V_{BE} = V_T \ln\left(\frac{I_C}{J_S A}\right) = \frac{kT}{q}\ln\left(\frac{I_C}{J_S A}\right) \tag{3.1}$$

where I_C is the collector current, $V_T = \frac{kT}{q}$ is the thermal voltage, J_S is the saturation current density, k is Boltzman's constant, q is the electron charge, A is the emitter area and T is the absolute temperature. Using (3.1), the difference of the base-emitter voltages of two BJT transistors, Q_1 and Q_2, can be written as

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{A_1 J_s}\frac{A_2 J_S}{I_{C2}}\right) = \frac{kT}{q}\ln\left(\frac{I_{C1}}{A_1}\frac{A_2}{I_{C2}}\right) \tag{3.2}$$

where I_{C1} and I_{C2} are the collector currents of transistors Q_1 and Q_2, respectively. Equation (3.2) shows that the difference of two base-emitter voltages is proportional to the absolute temperature.

Figure 3.1 shows a PTAT current reference circuit using the difference of two base-emitter voltages [19]. Transistors M_1 and M_2 form a current mirror, developing equal currents for transistors Q_1 and Q_2, i.e., $I_1 = I_2$. Following Kirchhoff's voltage law and equation (3.1), one can write

$$I_1 R = V_{EB2} - V_{EB1} = \frac{kT}{q}\ln(\frac{I_2}{A_2}\frac{A_1}{I_1}). \tag{3.3}$$

The current through M_5 must then be

$$I_{PTAT} = \frac{kT}{qR}\frac{(W/L)_5}{(W/L)_1}\ln(n) \tag{3.4}$$

where $n = \frac{A_1}{A_2}$ is the emitter-area ratio of Q_1 to Q_2 (A_1 is larger than A_2). One advantage of the PTAT current source in Figure 3.1 is that the current generated by this reference is, as a first approximation, independent of the power supply voltage. One drawback of this circuit is that it has an additional stable operating point, which is when I_1 is equal to zero. A start-up circuit is required to prevent the circuit from

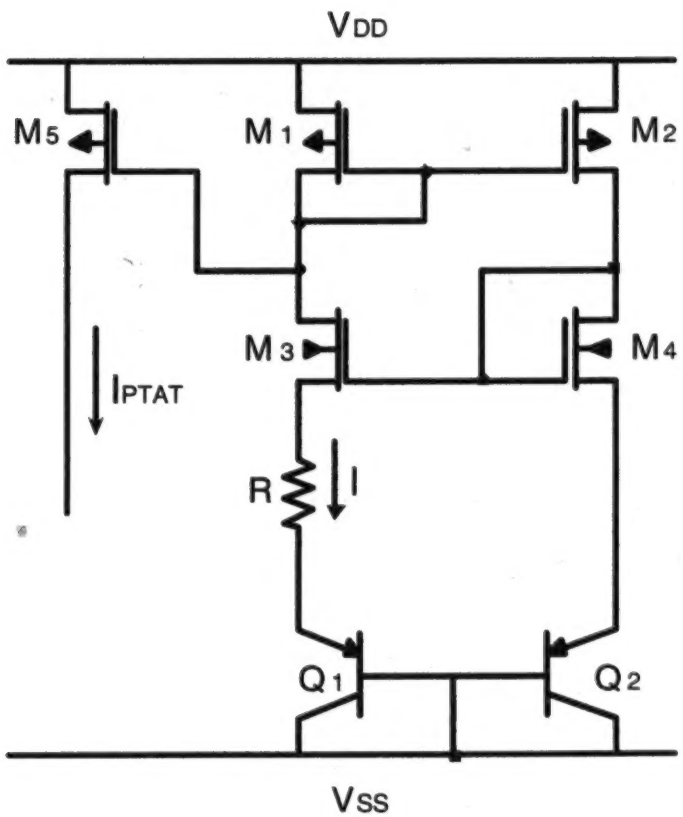


Figure 3.1: PTAT current generator (after [19])

settling in this state. Basically, the start-up circuit eliminates a possible zero current condition by injecting current at a suitable node and forces the circuit to move from the zero state to the correct point of operation [17].

In a conventional CMOS process, the necessary bipolar transistors can be realized using the substrate as part of the transistor. They can be fabricated with the substrate acting as the collector, the well diffusion as the base and the source/drain diffusion as the emitter (Figure 3.2). Since the collector is the substrate, n-well technology can be used for the realization of *pnp* transistors and p-well technology permits the realization of *npn* transistors [17].

PTAT currents can also be implemented using pure CMOS transistors. Figure 3.3 shows one possible pure CMOS design for the implementation of PTAT current generator [1]. The mirror block with mirroring factor equal to 1, provides equal currents in each branches. Using KVL for the voltage loop consisting of transistors M_1 and M_2 and resistor R, one can write

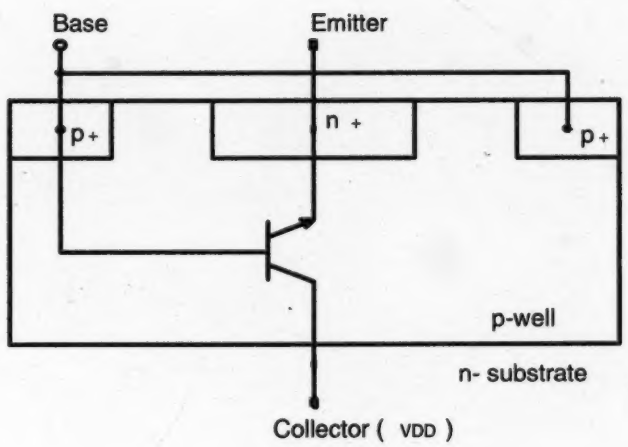
$$RI = V_{GS1} - V_{GS2} \tag{3.5}$$

and therefore, the following PTAT current, I_{PTAT}, is obtained

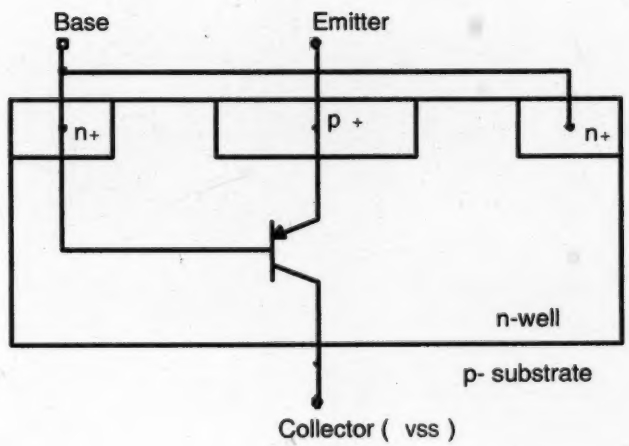
$$I_{PTAT} = I = \frac{V_{GS1} - V_{GS2}}{R} \tag{3.6}$$

The CMOS transistors, M_1 and M_2, should operate either in the subthreshold or saturation regions, so that the generated current becomes proportional to the absolute temperature. In what follows we describe the operation of the circuit in these two cases.

Subthreshold Region: In subthreshold region, a MOS transistor operates as a bipolar transistor and the current I_D changes exponentially with variations in V_{GS}, similarly to a bipolar transistor. The V_{GS} of a MOS transistor operating in the



(a)



(b)

Figure 3.2: (a) Substrate *npn* transistor (b) Substrate *pnp* transistor (after [3])

subthreshold region is given by [16]

$$V_{GS} = nV_T \ln\left(\frac{I_D}{(W/L)I_t}\right) + V_{TH} - nV_T \ln(1 - e^{\frac{-V_{DS}}{V_T}}) \tag{3.7}$$

where n and I_t depend on process parameters, W is the width of the transistor, L is the length of the transisto and V_{DS} is the drain-source voltage. Substituting (3.7) in (3.6), the PTAT current is found to be

$$I_{PTAT} = I = \frac{nV_T}{R} \ln\left(\frac{(W/L)_2}{(W/L)_1}\right), \tag{3.8}$$

which is proportional to the absolute temperature, T.

One drawback of this circuit, when the transistors M_1 and M_2 are operating in the subthreshold region, is that the temperature-range within the circuit can operate is limited. This is due to the presence of the leakage currents. The leakage currents have positive temperature dependency and increase as the temperature increases. Therefore, they can override the drain current of the MOS transistor operating in the subthreshold region at moderately high temperatures [1] and this affect the performance of the circuit.

Saturation Region: The same circuit can be used with the transistors working in the saturation region. In the saturation region the gate-source voltage of a MOS transistor is expressed as

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu C_{ox}(W/L)}}. \tag{3.9}$$

Substituting (3.9) in (3.6) and solving for I_{PTAT}, one can write [20]

$$I_{PTAT} = I = \frac{2}{\mu C_{ox} R^2} \left(\frac{1}{\sqrt{(W/L)_1}} - \frac{1}{\sqrt{(W/L)_2}}\right)^2. \tag{3.10}$$

We assume that R is a temperature-dependent resistor and its temperature dependence is expressed as $R = R_0(1 + \alpha_{R1}(T - T_0) + \alpha_{R2}(T - T_0)^2)$ where α_{R1} and α_{R2}

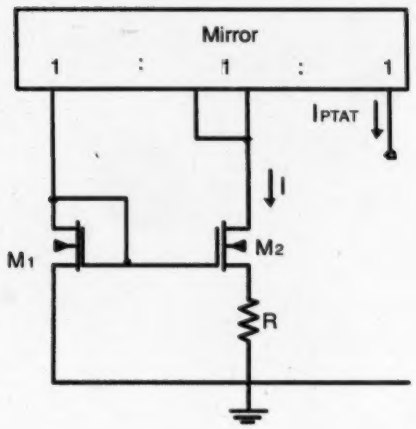


Figure 3.3: CMOS PTAT current generator (after [1])

are the first and second-order temperature coefficients of the resistor, R. Then, using equation (2.17) for the temperature dependence of the mobility, μ, the Taylor series of equation (3.10) is equal to

$$I_{PTAT} = \left(\frac{I_{PTAT0}}{R_0}^2\right)\{1 + (\frac{m}{T_0} - 2\alpha_{R1})(T - T_0) + \left(-2\alpha_{R2} + 3\alpha_{R1}^2 + \frac{m(m-1)}{2T_0^2} + \frac{m^2}{T_0^2} - \frac{2m\alpha_{R1}}{T_0}\right)(T - T_0)^2\} + O((T - T_0)^3) \tag{3.11}$$

where $I_{PTAT0} = \frac{2}{C_{ox}\mu_0 R_0^2}\left(\frac{1}{\sqrt{(W/L)_1}} - \frac{1}{\sqrt{(W/L)_2}}\right)^2$ and T_0 is the reference temperature. Using a first-degree approximation, the current I_{PTAT} can be written as

$$I_{PTAT} \simeq I_{PTAT0}(1 + \gamma(T - T_0)) \tag{3.12}$$

where $\gamma = (\frac{m}{T_0} - 2\alpha_{R1})$. Equation (3.12) shows that the temperature coefficient of the current I_{PTAT} can be controlled by the value of the α_{R1} and it will be positive if $\alpha_{R1} < \frac{m}{2T_0}$, which is usually the case.

A drawback of this circuit is that it has an additional stable operating point, similar to the circuit in Figure 3.1. Therefore, a start-up circuit is required to prevent

the circuit from settling in this unwanted state.

3.2 CTAT Current References

Another useful current reference is a reference that generates a current which is complementary-to-absolute temperature (CTAT). As we will see in the next chapter, this type of current reference is used in the design of bandgap voltage references. A simple method to generate a CTAT current is to force a CTAT voltage across a resistor. The base-emitter voltage of a bipolar transistor and the threshold voltage of a CMOS transistor are two voltages which have negative temperature coefficients and thus can be used for generating CTAT currents.

Figure 3.4 shows a possible design for the CTAT current generators using the base-emitter voltage. The amplifier ensures that the voltages at nodes A and B are equal. Therefore, the base-emitter voltage is forced across the resistor and a CTAT current is generated which is given by

$$I_{ref} = \frac{V_{EB}}{R}. \tag{3.13}$$

The temperature coefficient of the base-emitter voltage is equal to -2.2 mV/°C at room temperature [17]. The temperature coefficient of the resistor R should be so small that it can be neglected, so that the the current I_{ref} shows a negative temperature dependence.

The threshold voltage of a MOS transistor is another built-in voltage with negative temperature dependence and can be used for the design of CMOS CTAT current references. A possible design for such a circuit is shown in Figure 3.5. Transistors M_1 through M_5 form the threshold extractor [21]. Assuming matched transistors, so that each PFET transistor has the same threshold voltage, the voltage across the drain

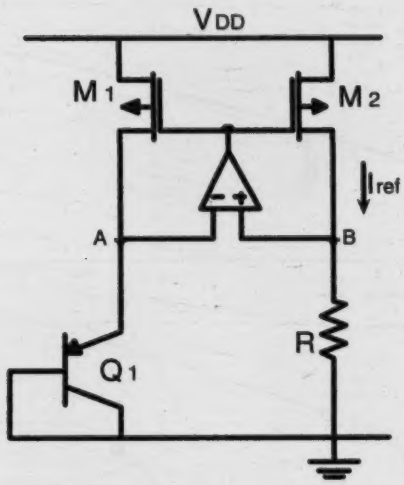


Figure 3.4: CTAT current generator using V_{BE} (after [17])

and source of transistor M_3 can be written as

$$V_{SD3} = V_{SG3} - V_{SD2}. \tag{3.14}$$

If transistor M_1 operates in saturation and M_2 in the triode region, then V_{SD2} is given by

$$V_{SD2} = \sqrt{2I}\left[\sqrt{\frac{1}{K_1} + \frac{3}{K_2}} - \sqrt{\frac{1}{K_1}}\right] \tag{3.15}$$

where $K_i = \mu_p C_{ox}(\frac{W}{L})_i, i = 1, 2, 3$. By making the width-to-length ratio of M_3, three times that of M_1 and M_2, i.e, $K_1 = K_2 = K_3/3$, and substituting (3.15) in (3.14), the drain-source voltage of transistor M_3 is expressed as

$$V_{SD3} = |V_{THp}| + \sqrt{\frac{6I}{3K_1}} - \sqrt{\frac{2I}{K_1} + \frac{6I}{K_1}} + \sqrt{\frac{2I}{K_1}} = |V_{THp}|. \tag{3.16}$$

This extracted threshold voltage is then buffered and applied to the resistor R to create the I_{CTAT} current which is given by

$$I_{CTAT} = \frac{|V_{THp}|}{R}. \tag{3.17}$$

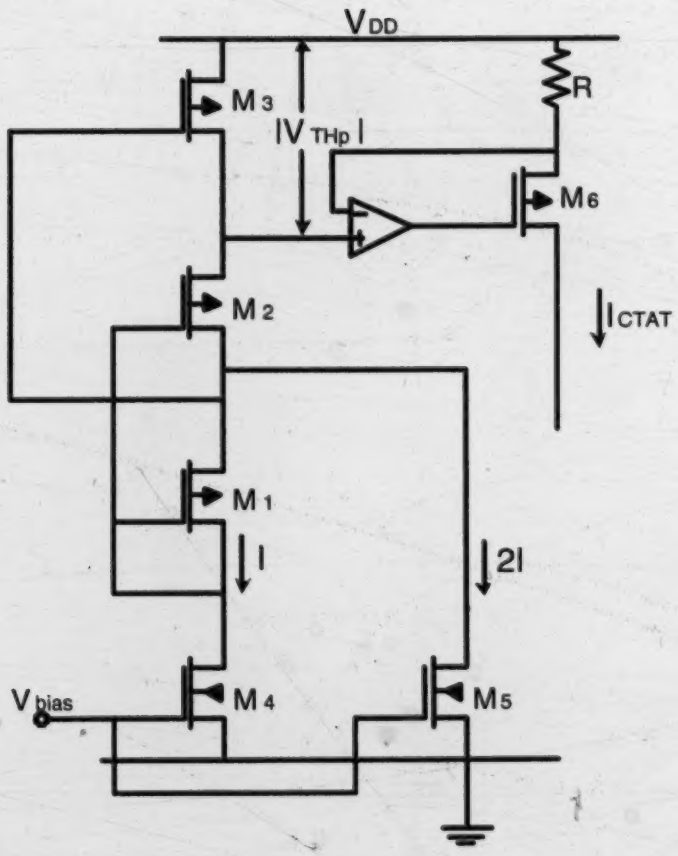


Figure 3.5: CMOS CTAT current generator using the threshold voltage (after [18])

One disadvantage of this circuit is that since the temperature coefficient of the threshold voltage is somewhat process-dependent, the behavior of the output current will dependent on the process as well. The temperature coefficient of the resistor should be small so that it will not affect the temperature behavior of the reference current.

3.3 Temperature-Independent Current References

Temperature-independent current generators are useful for biasing the circuits with fixed current densities across the desired temperature range. They are also used in the design of temperature-independent voltage references. One way to design a temperature-independent current reference is to add PTAT and CTAT currents appropriately. The sum of these currents usually will yield to a quasi-temperature independent current (to a first-order compensation). Figure 3.6 illustrates one possible design for summing the PTAT and CTAT currents. In this circuit, I_{PTAT} is generated by the loop consisting of transistors $Q1$ and $Q2$ and resistor $R1$ and the CTAT current is created by transistor $Q3$ and resistor $R2$. It is again assumed that the temperature coefficients of the resistors are very low. The PTAT and CTAT currents are then summed and a temperature-independent current is obtained.

Another method for the design of temperature-independent current generators is to use the circuit shown in Figure 3.3, when transistors M_1 and M_2 are operating in the saturation region. The operation of the circuit was discussed in previous section. According to (3.11), in order to achieve first-order compensation, the first-order temperature coefficient of the resistor should satisfy the following condition

$$\alpha_{R1} = \frac{m}{2T_0}. \tag{3.18}$$

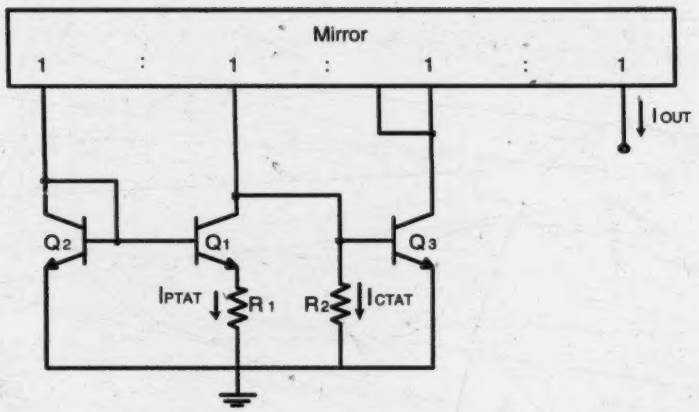


Figure 3.6: Temperature-independent current reference (after [1])

For second-order compensation, the second-order temperature coefficient of the resistor also should be equal to

$$\alpha_{R2} = \frac{m}{2T_0^2}(1 - \frac{5m}{2}). \tag{3.19}$$

The third technique for the design of a temperature-independent current reference is to force a temperature-independent voltage across a resistor with a very small temperature coefficient. This technique requires a temperature-independent voltage reference, which is not easily implemented.

3.4 PTAT^2 Current References

PTAT^2 current references generate a current which is proportional to the square of the temperature. As we will see in the next chapter, this type of current reference can be used for the design of curvature-compensated voltage references. A simple method of implementing a PTAT^2 current reference is to force a PTAT voltage through a resistor which shows a PTAT dependence. This method however depends on the technology.

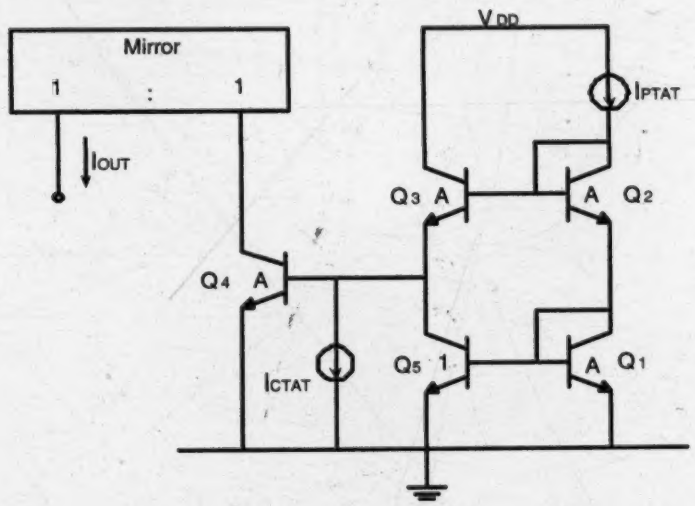


Figure 3.7: Bipolar PTAT^2 current reference (after [1])

Multiplier circuits can also yield in generating a PTAT^2. Figure 3.7 shows a PTAT^2 current reference designed with BJT transistors. Applying KVL for the loop consisting of transistors Q_1, Q_2, Q_3 and Q_4 and using equation (3.1) for each base-emitter voltage one can find that

$$I_{out} = I_{C4} = \frac{I_{C1}I_{C2}}{I_{C3}} = \frac{I_{PTAT}^2}{\frac{I_{PTAT}}{A} + I_{CTAT}} \tag{3.20}$$

where A is the emitter area of transistors Q_1-Q_4. If the circuit is designed in such a way that the sum of I_{CTAT} and I_{PTAT}/A will be equal in the desired temperature range, then I_{out} in equation (3.20) will be proportional to the square of the temperature.

Figure 3.8 illustrates a CMOS implementation for a PTAT^2 current generator. In this circuit, transistors M_1 and M_2 operate in subthreshold region, transistors M_3 in the saturation region and M_4 operates in the triode region. Using KVL for the voltage loop composed of transistors M_1, M_2 and M_4, the output current can be expressed

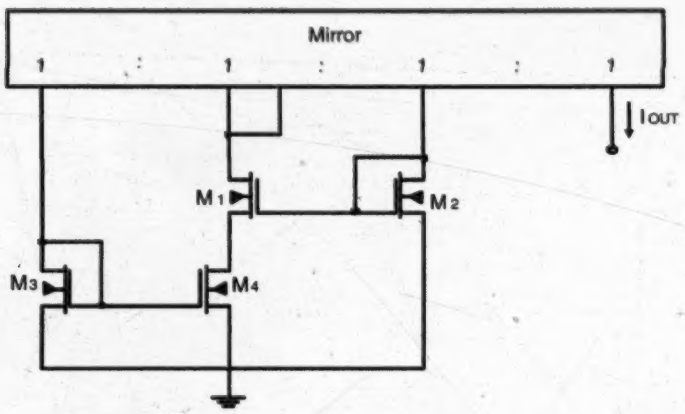


Figure 3.8: CMOS PTAT^2 current reference (after [1])

as

$$I_{D1} = \frac{V_{GS2} - V_{GS1}}{R_{DS4}} = \frac{nV_T}{R_{DS4}} \ln\left(\frac{(W/L)_1}{(W/L)_2}\right) \tag{3.21}$$

where R_{DS4} is the output resistance of transistor M_4 and is given by

$$R_{DS4} = \frac{1}{K_4(V_{GS4} - V_{TH})} \tag{3.22}$$

where $K_4 = \mu C_{ox}(\frac{W}{L})_4$. The mirroring factors, provided by the mirror block, are equal to 1. Therefore, I_{D3}=I_{D1}=I_{D2}=I_{out}. Also, since transistor M_3 operates in saturation one can write

$$V_{GS3} = V_{GS4} = V_{TH} + \sqrt{\frac{2I_{out}}{K_3}} \tag{3.23}$$

where $K_3 = \mu C_{ox}(\frac{W}{L})_3$. Using equation (3.21) and (3.22) the output current can be expressed as

$$I_{out} = \frac{2n^2K_4^2}{K_3} V_T^2 \ln^2\left(\frac{(W/L)_1}{(W/L)_2}\right). \tag{3.24}$$

$K_i, i = 3, 4$ depends on mobility. If in a technology the mobility parameter m is small and the mobility could be considered constant over the desired temperature range, the current I_{out} would be proportional to the square of the temperature.

3.5 Conclusion

Current references are essential building blocks of analog and digital circuits. The circuits designed for current processing operate at higher speed compare to their counterpart voltage-based implemented circuits. The current also influences the power consumption and static and dynamic properties of the circuit and therefore special attention should be paid to the design of the reference current generator.

The techniques used for the design of four different type of current references were studied in this chapter. A PTAT current reference generates a current proportional to temperature. It was shown that forcing a built-in PTAT voltage, such as the difference between the base-emitter voltages of two transistors, across a resistor can be used for generating a PTAT current. The current generated by a CTAT current reference, has a negative temperature coefficient. The threshold voltage of MOS transistor or the base-emitter voltage of a bipolar transistor can be used for the design of such reference. The proper combination of CTAT and PTAT current references results in a temperature-independent current. Finally the design methods used for generation of $PTAT^2$ current references were discussed. This type of current reference has applications in the design of precise voltage references.

Chapter 4

Voltage References

Voltage references find applications in a variety of circuits and systems including linear and switching regulators, Analog to Digital (A/D) and Digital to Analog (D/A) converters, voltage to frequency converters, power supply supervisory circuits, power converters and other circuits requiring an accurate reference voltage [17]. An ideal voltage reference must be, inherently, well-defined and its output voltage should be independent of temperature, power supply variations, load variations and other operating conditions.

As it was seen in the previous chapter, the design of most current references is based on forcing a voltage across a resistor. Integrated resistors have the tolerance on the order of 10 to 20% [1]. This tolerance directly translates to the overall tolerance of the current reference, making it difficult to realize precise integrated current references. But the accuracy of the voltage references, is typically higher and their output voltage is more predictable, forcing the circuit designers to prefer them to current references.

This chapter discusses the theory and issues, with respect to temperature, that surround the design of a voltage reference. A voltage reference can be categorized

into different performance levels (i.e., zero-order, first-order, or second-order). Zero-order references usually are designed using a Zener or a forward-biased diode and typically are not temperature compensated and will not be discussed here. For the first-order voltage references, the first-order term of the polynomial relationship of the output voltage with respect to temperature is canceled. Second-order as well as high-order voltage references, compensate one or more higher-order temperature dependent terms. These accurate voltage references are used for applications such as high-performance data converters and low-voltage power supply systems [1].

The chapter starts with a section on the design of the most popular voltage references, i.e., the bandgap voltage references. The basic idea of the design of a bandgap reference will be followed by a review on the history of its development. Then the techniques which are used for the design of first-order, second-order and low-voltage low-power bandgap references will be studied.

The bandgap voltage reference is bipolar in nature and when the supply voltage is below the bandgap voltage, i.e., about 1.2V, a conventional bandgap reference does not operate well [5], [22]. Therefore IC designers are challenged with designing circuits that can be implemented in low cost CMOS technology and with performance comparable to the performance of the bandgap voltage references. The methods which are used for the design of non-bandgap CMOS voltage references will be also studied.

4.1 Bandgap References

For many years, bandgap references have been used as voltage references in various fields of application, for instance in the automotive industry [23], battery-operated dynamic-random access memories (DRAMs) [24] and many other circuits. A bandgap

voltage reference has high power rejection and its output voltage is very stable against temperature and process variations.

All of the bandgap references used in this diversity of applications are based on the idea of Hilbiber in 1964 [25]. In his paper, he proposed to add and subtract several base-emitter voltages with different first-order behaviors for the temperature compensation of a base-emitter voltage. Because of using several base-emitter voltages, the required power supply voltage was large. In 1965, Widlar found a PTAT voltage by using the difference of two junction voltages [26]. In 1971, Widlar used this PTAT voltage for the compensation of the temperature behavior of base-emitter voltage in the design of a bandgap reference [27] which required a lower power supply compared to Hilbiber's proposal. Later, a number of articles describing several designs for the bandgap references appeared [28], [29], [30]. Most of the proposed topologies were based on Hilbiber or Widlar proposals or a combination of them. But all of the proposed references were only first-order compensated. In 1978, Widlar proposed a bandgap reference with an attempt for the second-order temperature compensation [31]. In his design he used different temperature behaviors for the collector currents generating the base-emitter voltages. Later on many high-order temperature compensation techniques, such as quadratic temperature compensation proposed by Song *et al.* [3], exponential temperature compensation developed by Lee *et al.* [32], piecewise-linear curvature correction presented by Rincon-Mora *et al.* [33], second-order curvature-compensated reference using resistor ratio designed by Lewis and Brokaw [34], were proposed.

Bandgap references started to be implemented in CMOS technology in the late seventies when weak-inversion MOS transistors became available [35]. A bipolar substrate transistor was used to generate the base-emitter voltage. Later on the

design of CMOS bandgap references was improved and parasitic BJTs were exploited in n-well and p-well [3],[4].

4.1.1 General Idea

By definition, a bandgap reference is a voltage reference of which the output voltage is referred to the bandgap energy of the used semiconductor. As it was discussed in Chapter 2, the bandgap energy has a weak temperature dependency. Therefore if the output voltage of a reference is referred to the bandgap voltage, a true reference voltage is obtained. (In the rest of this chapter, it is assumed that the bandgap voltage is constant over the desired temperature range and is equal to V_{G0}, the extrapolated bandgap voltage at 0°K,). For the realization of a bandgap reference, at least one component must be available of which a port voltage is related to the bandgap energy. Since the base-emitter voltage of a bipolar transistor is related to the bandgap energy, the bipolar transistor is the core component of most bandgap references. Bipolar transistors can also be implemented in CMOS technology using the substrate (Figure 3.2).

Following [36], we now obtain the relation between the base-emitter voltage and the bandgap energy. The base-emitter voltage, V_{BE}, of the bipolar transistor can be expressed as

$$V_{BE}(T) = \frac{kT}{q}\ln\left(\frac{I_C(T)}{I_s(T)}\right) \tag{4.1}$$

where T is the absolute temperature, q is the electron charge $(1.6 \times 10^{-19})C$, k is the Boltzmann constant $(1.38 * 10^{-23} J/K)$, $I_C(T)$ is the collector current and $I_S(T)$ is the saturation current. $I_s(T)$ is described as

$$I_S(T) = Dqn_i(T)^2 T^{1-n} \tag{4.2}$$

where D and n are constants and $n_i(T)$ is the intrinsic carrier concentration described by (2.2). Substituting (2.2) and (4.2) into (4.1) we obtain

$$V_{BE}(T) = \frac{kT}{q}\ln\left(\frac{I_C(T)}{qD'T^{\eta}}\right) + \frac{E_g}{q} = \frac{kT}{q}\ln\left(\frac{I_C(T)}{qD'T^{\eta}}\right) + V_{G0}. \tag{4.3}$$

In (4.3) $D' = DA^2$ and $\eta = 4 - n$ are constants. Now assume that the collector current, with which the transistor is biased, is described by

$$I_C(T) = I_{C0}\left(\frac{T}{T_0}\right)^{\theta} \tag{4.4}$$

where I_{C0} is the current at the reference temperature T_0, θ is the order of the temperature behavior of the current (for the constant current $\theta = 0$ and for the PTAT current $\theta = 1$). Using (4.4), equation (4.3) is simplified to

$$V_{BE}(T) = V_{G0} - [V_{G0} - V_{BE}(T_0)]\frac{T}{T_0} - \frac{kT}{q}(\eta - \theta)\ln\left(\frac{T}{T_0}\right) \tag{4.5}$$

where $V_{BE}(T_0)$ is the base-emitter voltage at the reference temperature T_0. Equation (4.5) is depicted in Fig 4.1 for several values of θ. It can be seen that the temperature dependence of the base-emitter voltage is negative.

The basic idea of all the bandgap references is the same: Compensate the temperature dependency of the base-emitter voltage with a complementary voltage, V_{comp}, so that the sum of V_{BE} and V_{comp} becomes equal to V_{G0} over the total temperature range. The implementation, technology and the ways of compensation varies for different schems.

In equation (4.5), $(T.\ln T)$ is the nonlinear temperature dependence factor of V_{BE}. The Taylor series of $V_{BE}(T)$ is given by

$$V_{BE}(T) = a_0 + a_1T + a_2T^2 + a_3T^3 + ... + a_nT^n + O(T^n) \tag{4.6}$$

where $a_i, i = 0, \cdots, n$ are the Taylor series coefficients. First-order temperature compensation involves the cancellation of the term T while high-order temperature

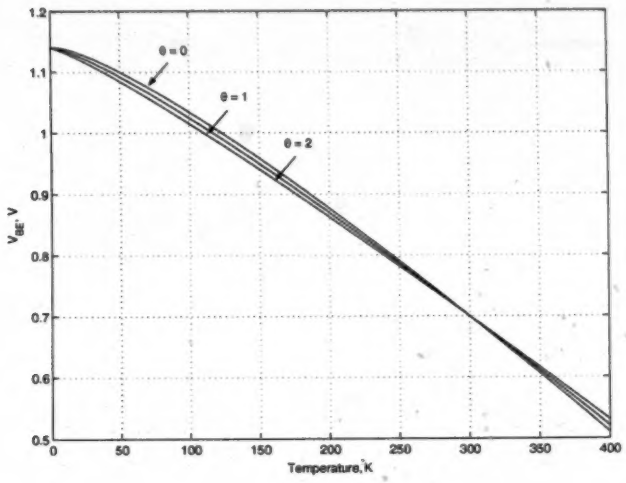


Figure 4.1: The base-emitter voltage as a function of temperature for several values of θ

compensation involves the cancellation of high-order T terms. The techniques which are used for the design of first-order bandgap references, is the topic of the next section.

4.1.2 First-Order Compensation

The thermal voltage $V_T = kT/q$ has a positive temperature coefficient equal to 0.086 mV/°C, and can be used for the first-order compensation of the temperature dependence of base-emitter voltage in the design of bandgap references. The coefficient, a_1 in equation (4.6) at room temperature is almost -2.2 mV/°C. Therefore, first-order temperature compensation at room temperature is obtained by properly combining V_{BE} and V_T, i.e.,

$$V_{REF} = V_{BE} + mV_T \tag{4.7}$$

where m is equal to $(2.2/0.086) = 25.6$ [17].

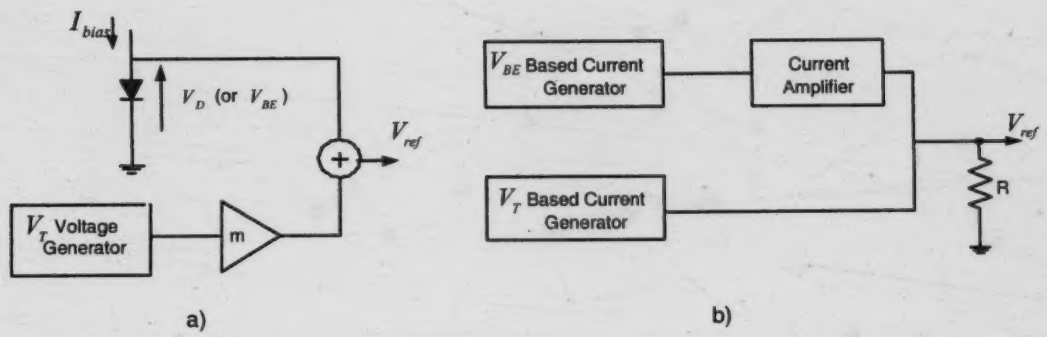


Figure 4.2: Two conceptual implementation of a temperature-compensated reference generator (after [17])

Most of the first-order bandgap references are implemented using one of the two techniques shown in Figure 4.2.

The first scheme directly implements equation (4.7), i.e, two voltages proportional to V_{BE} and V_T are added properly in order to obtain a temperature-independent reference. In the second method two currents, one proportional to V_{BE} and another one proportional to V_T, are properly scaled and summed up. The summed current, which is temperature-independent, will go through a resistor, generating a temperature-independent voltage. This configuration is also known as current-mode (CM) bandgap voltage reference [37].

To generate a voltage proportional to V_T, the base-emitter voltage difference of two bipolar transistor can be used. Using (4.1), the base-emitter voltage difference of two BJT transistors with two different emitter areas can be written as

$$\Delta V_{BE} = V_{BE1}(T) - V_{BE2}(T) = \frac{kT}{q}\ln\left(\frac{I_{C1}}{A_1 J_s(T)}\frac{A_2 J_s(T)}{I_{C2}}\right) = \frac{kT}{q}\ln\left(\frac{I_{C1}}{A_1}\frac{A_2}{I_{C2}}\right) \quad (4.8)$$

where $J_s(T) = (I_s(T)/\text{Area})$ is the saturation current density and A_1 and A_2 are the

emitter areas of the two transistors.

Figure 4.3 shows an implementation of the bandgap reference using the voltage processing technique. The circuit operates as follow: Transistors M_3 and M_4 form a current mirror which defines a given ratio between the currents in Q_1 and Q_2 (normally the mirror factor is 1). The operational amplifier and the associated feedback loop drives the voltages of nodes 1 and 2 to an equal value (i.e., V_{EB2}). Thus, the voltage drop across the resistor R_1 is equal to the base-emitter voltage difference of transistor Q_2 and transistor Q_1. Current I_1 is given by

$$I_1 = \frac{\Delta V_{EB}}{R_1} = \frac{V_T}{R_1} \ln\left(\frac{I_2}{A_2}\frac{A_1}{I_1}\right) \tag{4.9}$$

where A_1 and A_2 are the emitter areas of transistors Q_1 and Q_2, respectively. The output voltage, V_{ref}, is given by

$$V_{ref} = R_2 I_2 + V_{EB2}. \tag{4.10}$$

When the mirroring factor is 1, the currents I_1 and I_2 are equal and are given in equation (4.9). Substituting (4.9) in (4.10), V_{ref} can be written as

$$V_{ref} = R_2 \frac{V_T}{R_1} \ln\left(\frac{A_1}{A_2}\right) + V_{EB2}. \tag{4.11}$$

Therefore, for first order compensation, the resistor ratio, R_2/R_1 and the ratio of the emitter areas, A_1 and A_2, should satisfy

$$a_1 + \frac{kR_2}{qR_1} \ln\left(\frac{A_1}{A_2}\right) = 0, \tag{4.12}$$

where a_1 is the first-order temperature coefficient of V_{BE} in (4.6).

Figure 4.4 shows an implementation of a current-mode bandgap reference. Transistors M_3-M_5 form the current mirror with the mirroring factor equal to 1. The operational amplifier drives the voltages of nodes 1 and 2 equal to V_{EB2}. Therefore,

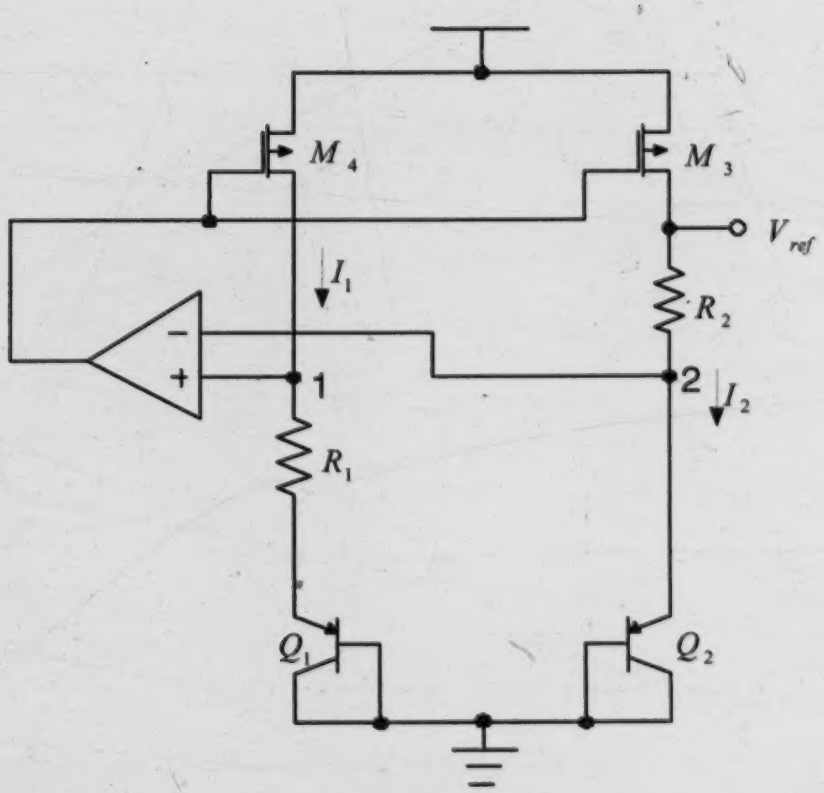


Figure 4.3: Typical CMOS bandgap reference based on voltage processing (after [38])

the voltage across the resistor R_1 is equal to the emitter-base voltage difference of transistors Q_2 and Q_1 and the current I_1 will be proportional to V_T and is given by

$$I_1 = \frac{V_{EB2} - V_{EB1}}{R_1} = \frac{V_T}{R_1} \ln\left(\frac{A_1}{A_2}\right). \tag{4.13}$$

The emitter-base voltage of transistor Q_2, across the resistor R_2, generates current $I_2 = \frac{V_{EB}}{R_2}$, with negative temperature coefficient. The sum of currents I_1 and I_2 is then equal to

$$I_1 + I_2 = \frac{kT}{qR_1} \ln\left(\frac{A_1}{A_2}\right) + \frac{V_{EB}}{R_2}. \tag{4.14}$$

The temperature behavior of V_{BE} is given in (4.6). If

$$\frac{a_1}{R_2} + \frac{k}{qR_1} \ln\left(\frac{A_1}{A_2}\right) = 0 \tag{4.15}$$

then $I_1 + I_2$ will be temperature-independent to a first approximation. This current is flowed into resistor R_3, generating a first-order temperature compensated voltage, V_{ref}, which is equal to

$$V_{ref} = V_{EB} \frac{R_3}{R_2} + V_T \frac{R_3}{R_1} \ln\left(\frac{A_1}{A_2}\right). \tag{4.16}$$

Note that all the resistors should be made from the same material to ensure compensation of the temperature coefficient.

As equation (4.16) shows, the circuit can easily achieve a gain or attenuation of the generated bandgap voltage by scaling the value of resistor R_3. This will affect the value of minimum required power supply for the circuit to operate.

The transistors forming the current mirror in the circuits shown in Figures 4.3 and 4.4 should operate in the saturation region. Thus, the minimum supply voltage must be maintained in order to prevent the transistors M_3-M_5 from being forced to operate in triode region. Therefore, for both circuits, the minimum required power supply is expressed by

$$V_{DD_{\min}} = V_{ref} + V_{SDsat}. \tag{4.17}$$

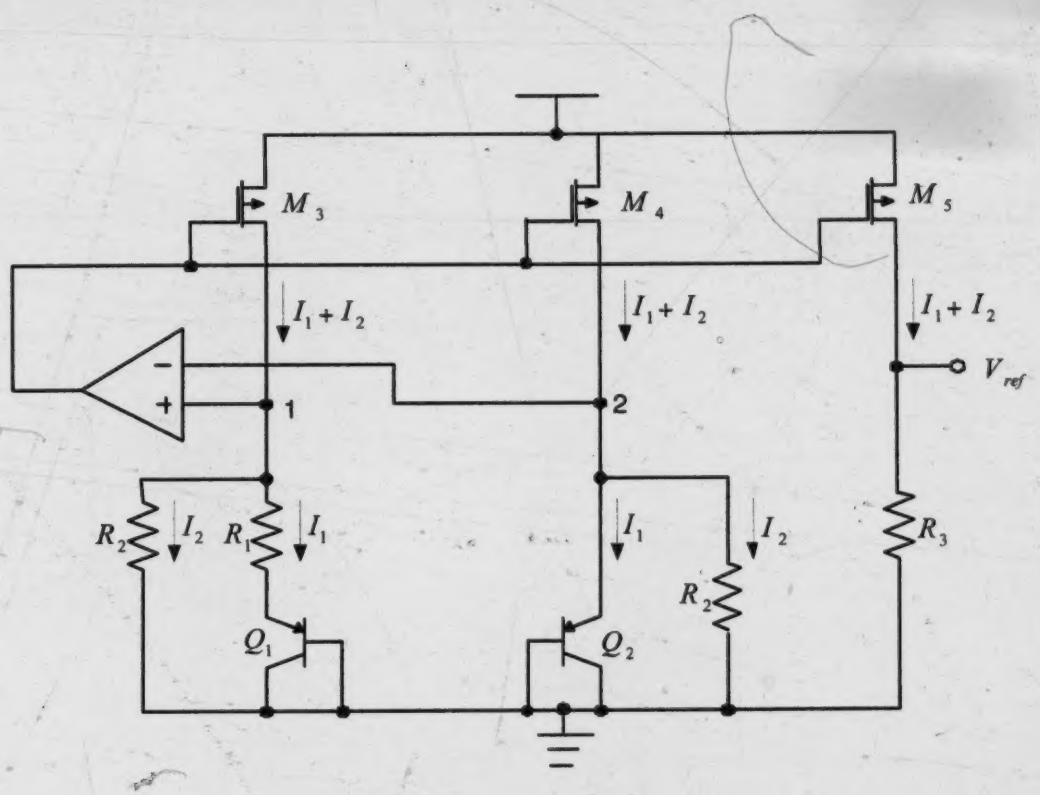


Figure 4.4: Typical CMOS bandgap reference based on current processing (after [17])

For the circuit in Figure 4.3 the typical value for V_{ref} is $1.25V$ and the value of V_{SDsat} ranges from $0.1V$ to $0.3V$. Thus, the theoretical value for the minimum required power supply is $1.4V$. However, since V_{ref} can be scaled down for the CM bandgap reference, the circuit in Figure 4.4 can be designed with a lower power supply compared to a bandgap reference based on voltage processing.

Offset is one of the main concerns in the design of bandgap references. In the circuits shown in Figures 4.3 and 4.4, the operation of the Op-Amp is to keep the voltages of nodes 1 and 2 to an equal value. This is generally true if the gain of the operational amplifier is sufficiently large. However, in real circuits, a possible offset always exists though it can be minimized with suitable cell design. In both circuits of Figures 4.3 and 4.4, considering the systematic offset voltage of V_{OS}, the current

I_1 is defined by the condition

$$\triangle V_{EB} + V_{OS} = R_1 I_1. \tag{4.18}$$

If the value of the offset is comparable to the value of $\triangle V_{EB}$, then the offset will significantly affect the performance of the circuit. One way to reduce the effect of V_{OS} on V_{ref} is to increase the value of $\triangle V_{EB}$. This can be done by increasing the ratio (A_1/A_2) in equation (4.9) or (4.13), e.g., replacing the single BJT transistors with an array of bipolar transistors. Laser trimming is another option but it is a costly solution.

The circuits described so far are designed to compensate the first coefficient of the temperature-dependence of V_{BE}. Due to the presence of high-order temperature coefficients, the output voltage is not precise. The design of second-order temperature compensated BGR is discussed in the next section.

4.1.3 Second-Order Compensation

Typical first-order bandgap references are not adequate for high-performance systems such as data and power converters. Therefore, higher-order references are in great demand for such precise applications and this has been resulted in the development of many high-order temperature compensation techniques [3], [32],[33],[34],[39]. Since first-order references only compensate the linear term, thereby leaving the characteristic curvature-variation across temperature, higher-order references are also known as curvature-corrected references. Several approaches have been suggested for curvature correction. One straightforward solution is to make the quantity $(\eta - \theta)$ in equation (4.5) equal to zero. In this case, there would be no nonlinear temperature-dependent term in (4.5). This could be achieved by using a very strongly temperature-dependent bias current. But the design of high-order temperature dependent current

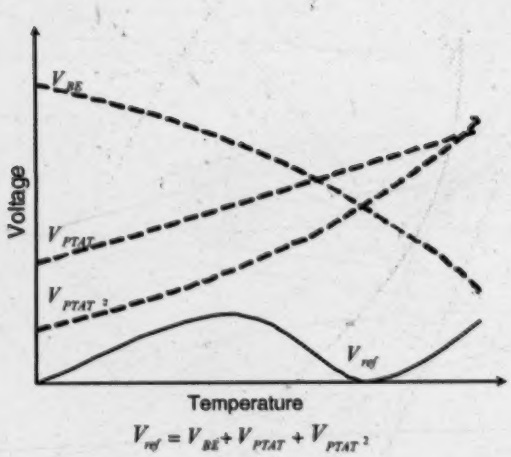


Figure 4.5: Curvature-compensation concept using a PTAT^2 voltage (after [1])

sources could be complicated. The basic idea behind the design of many curvature-compensated references is to simply add a curvature-correcting component which increases with temperature in a nonlinear fashion. In this section, we review some of the techniques based on this approach that are used for the design of curvature-compensated bandgap references.

4.1.3.1 Curvature Compensation Using Squared PTAT Voltage

The design of many precise BGRs are based on the cancellation of the second-order term in the Taylor-series expansion of the base-emitter voltage (equation (4.6)). The classical method for doing such compensation is through the addition of a squared PTAT voltage, to the output voltage relation of a first-order bandgap reference [1]. Figure 4.5 shows the concept of curvature compensation achieved by adding a PTAT^2 to the first-order temperature compensated BGR. Since the PTAT^2 term is small for the first-half of the temperature range, the output waveform shows the curvature of a first-order bandgap reference. However, as the temperature increases the squared

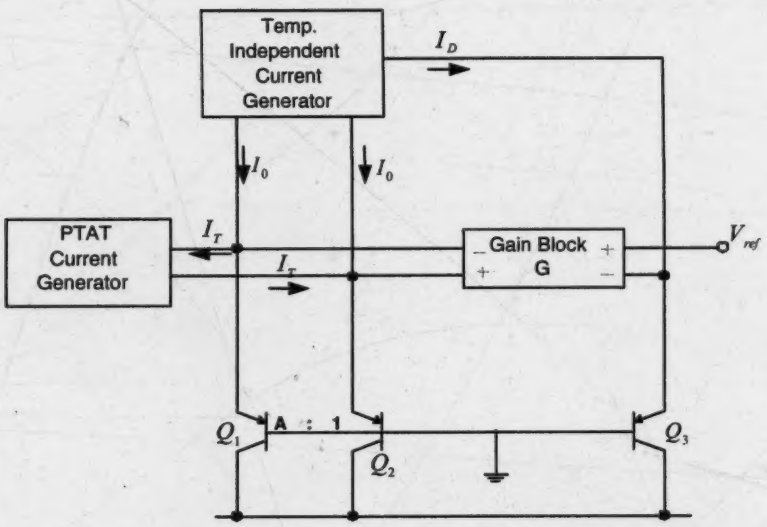


Figure 4.6: Schematic of the curvature-compensated BGR using square PTAT voltage compensation (after [3])

PTAT term becomes considerably large and is used to cancel the increasingly negative temperature dependence of the base-emitter voltage. Consequently, the curvature depicted by V_{ref} in Figure 4.5 results.

One implementation of this technique is illustrated in Figure 4.6 [3]. The current I_0 and the bias current I_D shown in this figure are temperature-independent and the PTAT current I_T is given by

$$I_T = \alpha V_T + \beta \tag{4.19}$$

where α and β are constant coefficients. The output voltage, V_{ref}, can be expressed as

$$V_{ref} = V_{EB3} + G(V_{EB2} - V_{EB1}) = V_{EB3} + G \triangle V_{EB} \tag{4.20}$$

where

$$\triangle V_{EB} = V_T \ln\left(A\frac{I_0 + I_T}{I_0 - I_T}\right), \tag{4.21}$$

A is the emitter area ratio of Q_1 and Q_2 and G is the gain. The Taylor series expansion of equation(4.21) will result in

$$\triangle V_{EB} = V_T \ln A + 2V_T \left(\frac{I_T}{I_0}\right) + \frac{2}{3}V_T \left(\frac{I_T}{I_0}\right)^3 + O\left((\frac{I_T}{I_0})^4\right) \tag{4.22}$$

Substituting (4.19) into (4.22), and neglecting higher order terms, (4.20) can be written as

$$V_{ref} = V_{EB3} + GV_T \ln A + G\frac{2\alpha}{I_0}V_T^2 + V_E \tag{4.23}$$

where V_E is the error voltage and is less than 1 mV at room temperature [3]. As it can be seen, a PTAT^2 voltage is appeared in equation (4.23). The temperature dependence of V_{EB3} is given by (4.6). If $a_2 + G\frac{2\alpha}{I_0} = 0$, then second-order temperature compensation is obtained. The experimental results show an average temperature drifts of 13.1 and 25.6 ppm/°C over the commercial and military temperature ranges, respectively.

4.1.3.2 Curvature Compensation Using Temperature-Dependent Resistor Ratio

Another technique for the cancellation of high-order components of the base-emitter voltage is to generate the nonlinear component by exploiting the temperature-dependence of different resistors in a given process technology [1].

Figure 4.7 shows a circuit implemented based on this technique, where the temperature coefficient of different resistors is used to compensate the higher-order components present in a first-degree bandgap cell [39]. In this circuit, resistors R_1, R_2 and R_4 are implemented using the same material and resistor R_3 is implemented by a different material.

The PTAT current, I, is generated by transistors Q_1, Q_2 and resistor R_1 and is

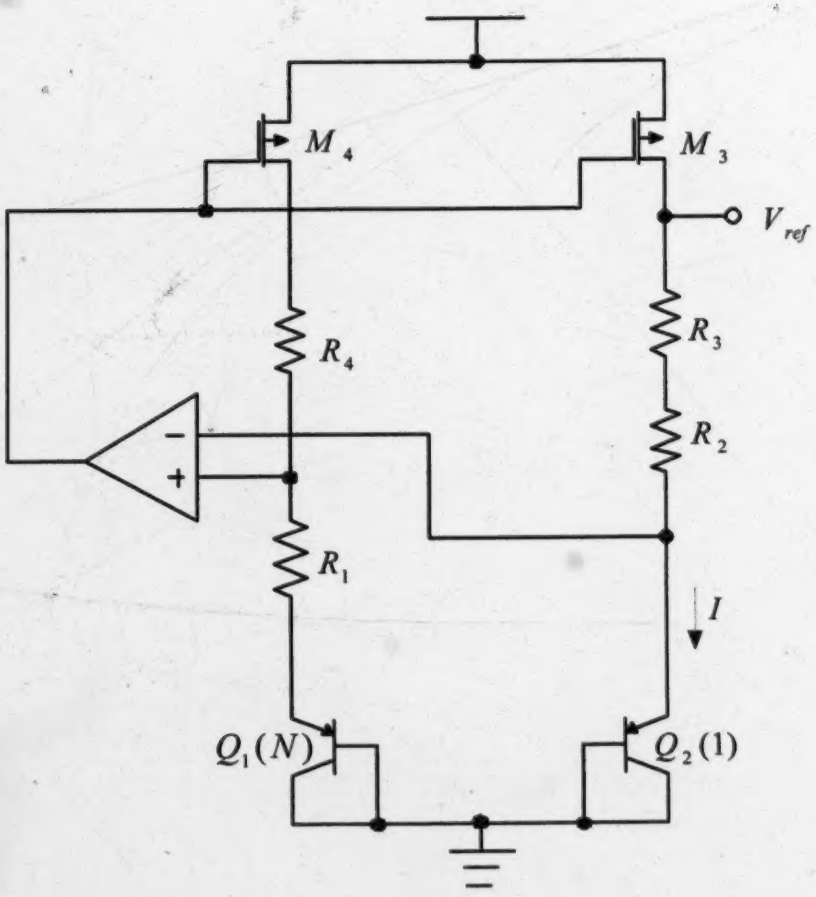


Figure 4.7: Schematic of the curvature-compensated BGR based on resistor ratio technique (after [39])

given by

$$I = \frac{V_T \ln(N)}{R_1} \tag{4.24}$$

where N is the emitter-area ratio of Q_1 and Q_2. The current I is passed through resistors R_2 and R_3 and so the output voltage V_{ref} is expressed as

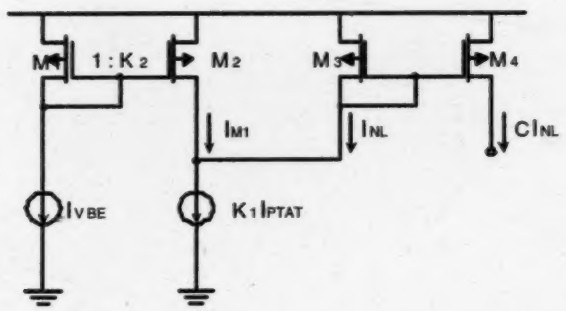
$$V_{ref} = V_{EB2} + \left[\frac{R_2}{R_1}\ln(N)\right] V_T + \left[\frac{R_3}{R_1}\ln(N)\right] V_T. \tag{4.25}$$

The resistor ratio R_2/R_1 is temperature-independent since both resistors are implemented by the same material. However, the ratio R_3/R_1 is temperature-dependent due to material difference and so the third term in equation (4.25) generates the desired nonlinear component which leads to curvature-compensation of the output voltage. For the temperature trimming, an optimum R_3/R_1 should be found such that the nonlinear error voltage becomes minimum. Then, the linear temperature dependence of the output voltage should be minimized by finding an optimum R_2/R_1. Experimental measurements show an average temperature drift of 5.3 ppm/°C in the temperature range of 0°C-100°C [39].

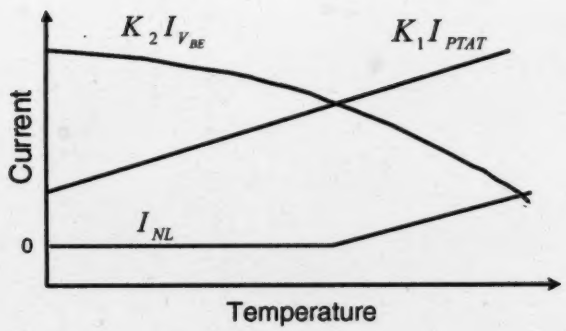
The advantages of this technique over using typical PTAT^2 are simplicity and cost effectiveness. Only one additional resistor is required to convert a first-order bandgap reference into a second-order circuit. However, there is one significant disadvantage. The performance of the circuit is highly dependent on the process and the temperature characteristics of the resistor ratio, (R_3/R_1), which vary substantially from process to process due to the inherent differences in technology [1].

4.1.3.3 Curvature Compensation Using Nonlinear Currents

A nonlinear current can also be used for generating the curvature-correcting component. This nonlinear current can be exponential [32] or piecewise linear [33]. Figure 4.8 shows a circuit used for generating a piecewise-linear current [33]. Transis-



(a)



(b)

Figure 4.8: Generation of the non-linear current (a) The circuit, (b) Currents (after . [33])

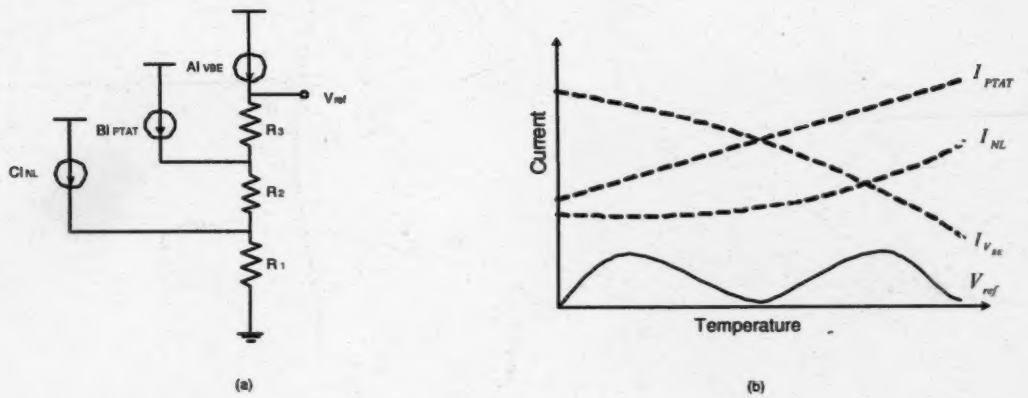


Figure 4.9: Piecewise-linear curvature-corrected bandgap reference a) The circuit b) Temperature-dependent waveforms (after [33])

tor M_2 is biased with $K_1 I_{PTAT}$ current.For the first lower half of the temperature, (when $K_2 I_{VBE} < K_1 I_{PTAT}$), transistor M_2 is forced to operate in the triode region ($I_{M1} = K_1 I_{PTAT}$). Consequently, M_3 does not conduct any current and I_{NL} is equal to zero. For the upper half of the temperature range, $K_1 I_{PTAT}$ becomes larger than the $K_2 I_{VBE}$. Therefore, M_2 becomes saturated and supplies $I_{M1} = K_2 I_{VBE}$, forcing M_3 to source the difference of $K_2 I_{VBE}$ and $K_1 I_{PTAT}$. The resulting current I_{NL} is nonlinear and can be described by

$$I_{NL} = \begin{cases} 0 & (I_{V_{BE}} \geq I_{PTAT}) \\ \\ K_1 I_{PTAT} - K_2 I_{V_{BE}} & (I_{V_{BE}} < I_{PTAT}) \end{cases} \tag{4.26}$$

where K_1 and K_2 are constants defined by the ratios of the mirroring transistors defining I_{PTAT} and $I_{V_{BE}}$.

Curvature correction can be obtained by combining the three temperature-dependent currents, I_{VBE}, I_{PTAT} and I_{NL}. A simple BGR circuit based on this approach is shown

in Figure 4.9(a)[33]. For this reference, the output voltage is given by

$$V_{ref} = AI_{VBE}[R_1 + R_2 + R_3] + BI_{PTAT}[R_1 + R_2] + CI_{NL}R1. \qquad (4.27)$$

The typical behavior of the output voltage of the circuit in Figure 4.9(a) is shown graphically in Figure 4.9(b). For the lower half of the temperature range, the current I_{NL} is equal to zero and the circuit behaves essentially like a first-order bandgap reference. For the upper half of the temperature range, the combination of the three currents diminishes the nonlinear effect of the base-emitter voltage. Experimental measurements show an average temperature drift of 20 ppm/°C in the temperature range of (-15-90)°C [33].

4.1.4 Low-Voltage Low-Power Bandgap References

In recent years, low power design is attracting much attention due to the emerging needs for battery-powered portable devices and systems. With the systems emphasis on low-power operation, the supply voltage is typically much lower than the nominal supply voltage for the process and is often defined by the minimum voltage of a battery [40]. According to the International Technology Roadmap for Semiconductors [41], in the year 2010, the mainstream supply voltage will be around 0.6 V. However, since the output voltage of the conventional BGR is 1.25, which is nearly the same voltage as the bandgap of silicon, the minimum power supply voltage needs to be greater than 1 V. Several approaches have been proposed to overcome this problem. In what follows, we will review some of the major methods used for the design of low-voltage low-power bandgap references.

A straightforward solution for low-voltage BGR design is to make the output voltage of the bandgap reference less than the bandgap of the silicon. One way to

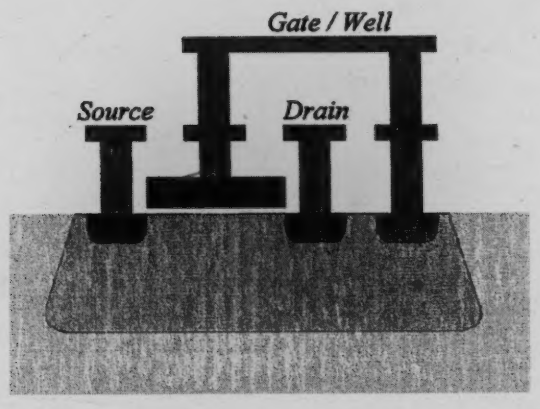


Figure 4.10: Cross section of a DTMOS transistor(after [40])

achieve this, is to use a low-bandgap material (e.g., germanium) for the diodes in the bandgap reference circuit. However, this option is expensive and is not available in a standard CMOS process [40]. As it was shown earlier, the output voltage of bandgap references using current processing can become lower than 1.25 V due to the presence of resistor ratios in equation (4.16). Therefore the second solution could be the use of a fraction of the voltage across the diodes by resistive subdivision [4], [5], [38] and [42]. However, the method of resistive subdivision requires a number of resistors, which need to be high-resistance for low-power applications. This will result in considerable area consumption.

A third technique for low-power, low-voltage bandgap reference design is to virtually lower the material bandgap, using an electrostatic field. To implement this method one has to replace the normal diodes by dynamic threshold MOS transistors (DTMOST) as it is proposed in [40].

A cross-section of DTMOST is shown in Figure 4.10. As it can be seen, this device is basically a MOS transistor with an interconnected body and gate and its operation is similar to weak-inversion MOS operation. This device can be looked upon in two

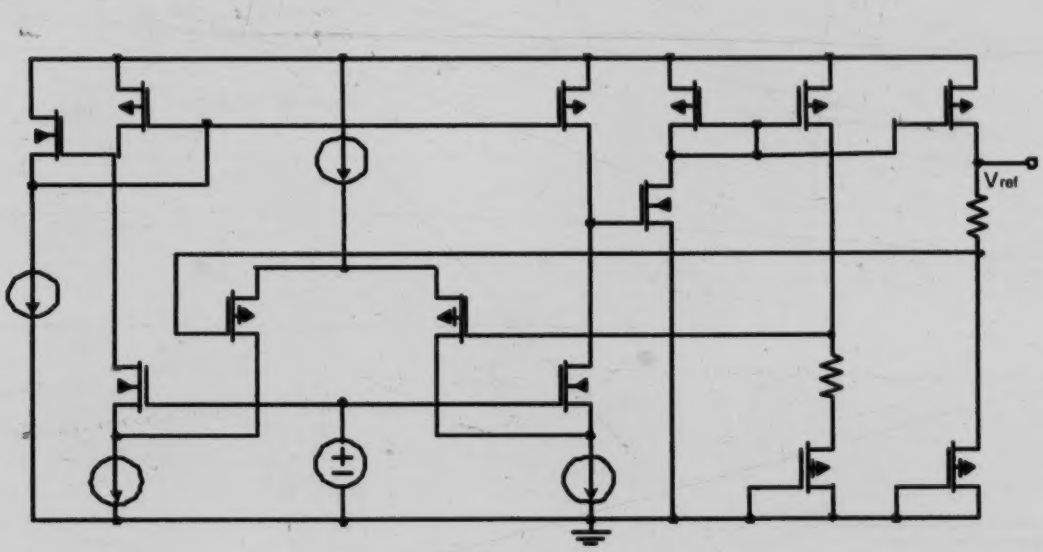


Figure 4.11: Low-voltage bandgap circuit schematic using DTMOS transistors (after [40])

ways. First, it can be seen as a lateral bipolar transistor with an extra gate over the base, and second, it can be viewed as a MOS whose threshold voltage is dynamically controlled by the V_{gs} voltage. The apparent material bandgap in the DTMOS is given by

$$V_{gap,apparent} = V_{gap0} - \phi_{b1} \tag{4.28}$$

where ϕ_{b1} is the barrier lowering voltage. This apparent bandgap can be approximated by a constant (the apparent material bandgap extrapolated to 0 K) which has been reported to be equal to 0.6 V for a standard 0.35-μm technology and a linearly temperature dependent term [40]. A DTMOS bandgap reference can be designed using the same topology of a conventional CMOS BGR. Figure 4.11 shows an example of such circuit. The DTMOS diodes are shown with the gate-backgate connection. The input stage of the folded cascode opamp is also implemented with DTMOS transistors which allows operation at low supply voltages. A low voltage current

mirror is used for the output stage of the opamp. The experimental results show that the output voltage and the minimum required power supply for the circuit are 0.65 V and 0.85 V, respectively. The variation of the output voltage over the temperature range of -25°C to 100°C is 57 ppm/°C. Nevertheless, this method of low voltage BGR design has a number of drawbacks. The DTMOS transistors require a large layout and have a large gate capacitance. Also, DTMOS is a non-standard device and this makes the circuit less reproducible.

4.2 CMOS non-Bandgap Voltage References

In the previous sections we studied the theory and the techniques used for the design of bandgap voltage references. It was shown that the output voltage of a bandgap reference has high power rejection and a very small temperature coefficient and is stable against process variations. However, IC design is now dominated by low power, low voltage objectives, making CMOS the technology of choice. The bandgap voltage reference is bipolar in nature and so when the supply voltage is below $1V$ a conventional bandgap reference does not show good stability [5], [22] and [43]. Therefore, IC designers are challenged with designing circuits that can be implemented in low cost CMOS technology and their performances are comparable to the performance of the bandgap voltage references.

In this section, we discuss the methods used for the design of CMOS non-bandgap voltage references. The issues, with respect to temperature, that surround the design in each technique are also studied.

4.2.1 CMOS Voltage References Based on Threshold Voltage Subtraction

The first step to realize a voltage reference is to find a stable unit voltage, such as the bandgap voltage used in bandgap voltage references [6]. One typical parameter in CMOS process, is the threshold voltage. However, as it was discussed in Chapter 2, the threshold voltage is temperature dependent and cannot be used as a reference over a wide temperature range.

In a multi-threshold technology, where transistors with different threshold-voltages are fabricated, a subtraction of two threshold voltages may result in the cancellation of temperature-sensitive parameters of the threshold voltages. Therefore, threshold-voltage subtraction can be used for the design of CMOS voltage reference [6], [44]. The simplified structure of such voltage reference is shown in Figure 4.12. Similar structures can be used by NMOS transistors. Transistor M_1 has a larger threshold voltage than M_2. Assuming equal current for both transistors and using

$$V_{GS} = V_{TH} + \sqrt{\frac{I}{K}} \tag{4.29}$$

where $K = \sqrt{(\mu C_{ox}(W/L))/2}$, for a saturated MOS transistor, the reference voltage is given by

$$V_{ref} = |V_{GS1}| - |V_{GS2}| = |V_{TH1}| - |V_{TH2}| + \sqrt{I}\left[\frac{1}{\sqrt{K_1}} - \frac{1}{\sqrt{K_2}}\right]. \tag{4.30}$$

Considering all possible variations in (4.30), the temperature dependency of the reference voltage is given by

$$\begin{aligned}\frac{\partial V_{ref}}{\partial T} =& \frac{\partial(|V_{TH1}| - |V_{TH2}|)}{\partial T} + \frac{1}{2\sqrt{I}}\left(\frac{1}{\sqrt{K_1}} - \frac{1}{\sqrt{K_2}}\right)\frac{\partial I}{\partial T} \\ &+ \frac{\sqrt{I}}{2}\left(\frac{1}{\mu_2\sqrt{K_2}}\frac{\partial \mu_2}{\partial T} - \frac{1}{\mu_1\sqrt{K_1}}\frac{\partial \mu_1}{\partial T}\right).\end{aligned} \tag{4.31}$$

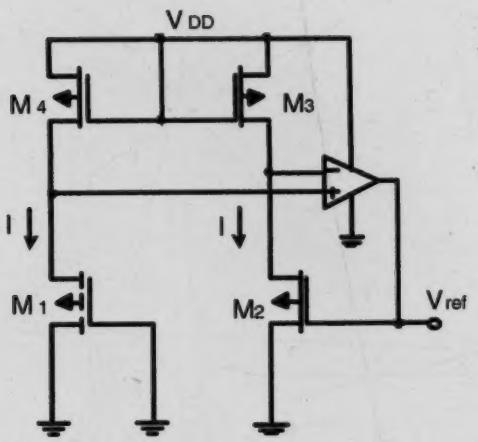


Figure 4.12: Schematic of the voltage reference based on threshold subtraction (after [43])

In (4.31), the drain current, the mobility, and the threshold voltage are the three temperature-dependent factors. The drain current varies with temperature because of its dependence on the threshold voltage and the mobility. If the transconductance parameters of two transistors are the same, i.e., $K_1 = K_2$, the effect of temperature variations of the drain current on the reference voltage will be eliminated. In practice, exact matching of transistor parameters may not be easy and a low bias current is generally used to minimize the effect of the drain current on the reference voltage. For further improvement of the temperature behavior of the reference voltage, the drain currents can be set at the ZTC point of the transistors, where they are independent of temperature [6]. In order to reduce the variation of the reference voltage due to the temperature dependence of the mobility, the absolute values of the mobilities of the transistors, as well as their temperature dependence, must be made the same [44].

Therefore, with proper circuit design and using a good process for the realization

of the transistors, the output voltage can be simplified to

$$V_{ref} \approx |V_{TH1}| - |V_{TH2}|. \tag{4.32}$$

A low temperature coefficient reference voltage is achieved with good process control that makes the TC of the threshold voltages of transistors M_1 and M_2 sufficiently close to each other.

In summary, this technique of implementing voltage references, requires: 1) extra fabrication steps to implement multi-threshold-voltage devices, 2) good process control to make temperature coefficient of the threshold voltages close to each other, and 3) preferably a temperature-independent low-magnitude bias current to improve the temperature behavior of the output voltage [45]. The temperature-dependence of the reference voltage is strongly affected by the process variation and bias current level. Another disadvantage of these references is that the output voltage is based on the threshold voltage and cannot be controlled accurately. However, this is of little importance rather than its temperature dependence since it can be adjusted by laser trimming or compensated by system design [44].

4.2.2 CMOS Voltage References Based on the Weighted Difference of Gate-Source Voltages

A CMOS voltage reference based on gate-source voltage difference between a PMOS and a NMOS transistor is presented in [46]. The main advantage of this reference is that it can be realized in a standard CMOS process.

The proposed circuit is shown in Figure 4.13. Transistors M_{s1}-M_{s3} form the start-up circuit. The bias circuit is similar to the circuit shown in Figure 3.3 and consists of transistors M_1-M_4 and resistor R_B. The bias circuit generates the bias current

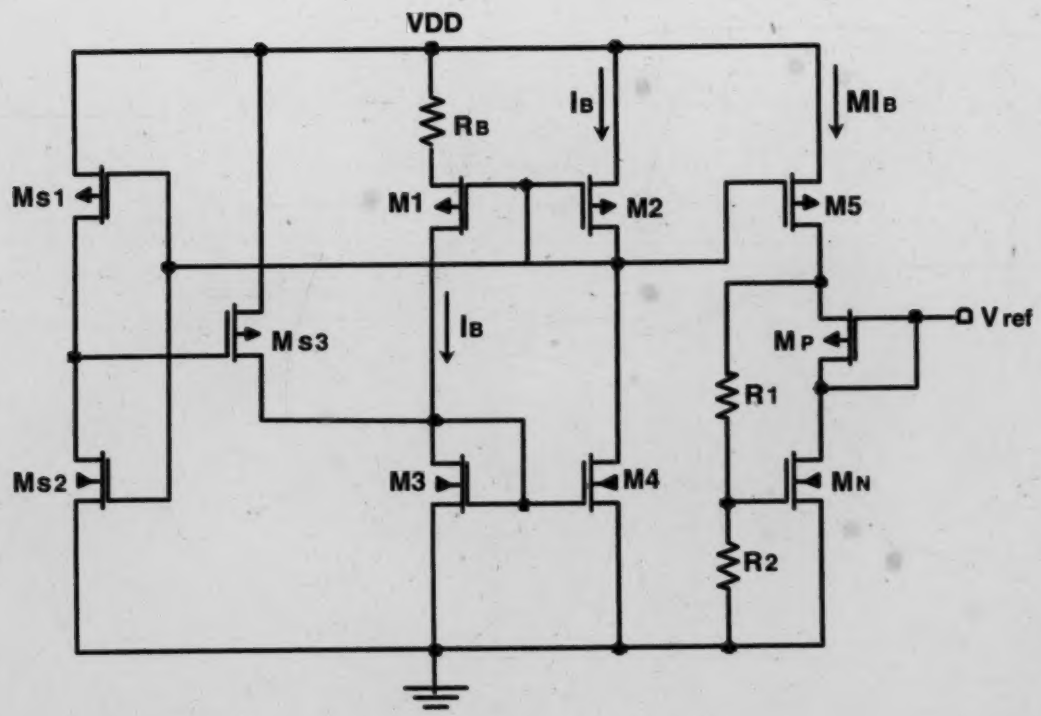


Figure 4.13: Schematic of the voltage reference based on weighted difference of gate-source voltages (after [46])

$I_B(T)$ which is given by

$$I_B(T) = \frac{2}{\mu_p(T_0)C_{ox}R_B^2}\left[\frac{1}{\sqrt{(\frac{W}{L})_2}} - \frac{1}{\sqrt{(\frac{W}{L})_1}}\right]^2 \left(\frac{T}{T_0}\right)^{m_p} = I_B(T_0)\left(\frac{T}{T_0}\right)^{m_p}. \quad (4.33)$$

The reference core circuit is formed by transistors M_N and M_P and resistors R_1 and R_2. From the circuit the reference voltage is given by

$$V_{ref} = \left(1 + \frac{R_1}{R_2}\right).V_{GSn} - |V_{GSp}|. \quad (4.34)$$

For proper operation of this circuit, all the transistors, especially M_P and M_N, should be biased in saturation. The temperature dependence of the output voltage is obtained by differentiating (4.34) with respect to the temperature. Using (4.29) for a saturated MOS transistor, the temperature coefficient of the reference voltage is given by

$$\begin{aligned}\frac{\partial V_{ref}}{\partial T} &= \left(1 + \frac{R_1}{R_2}\right)\frac{\partial V_{GSn}}{\partial T} - \frac{\partial |V_{GSp}|}{\partial T} \\ &= \left[-\left(1 + \frac{R_1}{R_2}\right)\alpha_{VTn} + \alpha_{VTp}\right] + \frac{m_p}{T_0}\sqrt{\frac{2MI_B(T_0)}{\mu_p(T_0)C_{ox}(\frac{W}{L})_p}} \\ &\times \left[\left(1 + \frac{R_1}{R_2}\right)\left(\frac{1}{2} + \frac{m_n}{2m_p}\right)\sqrt{\frac{\mu_p(T_0)(\frac{W}{L})_p}{\mu_n(T_0)(\frac{W}{L})_n}}\left(\frac{T}{T_0}\right)^{\frac{m_p+m_n-2}{2}} - \left(\frac{T}{T_0}\right)^{m_p-1}\right]\end{aligned} \quad (4.35)$$

where M is the mirroring factor (as shown in Figure 4.13), α_{VTn} and α_{VTp} are the temperature coefficients of the threshold voltages of PMOS and NMOS transistors, and m_p and m_n are the mobility exponents of PMOS and NMOS transistors, respectively. In order to obtain a temperature-independent output voltage, the linear term should be set to zero by the resistor ratio, which is given by

$$\frac{R_1}{R_2} = \frac{\alpha_p}{\alpha_n} - 1. \quad (4.36)$$

The high-order term can be set to zero at the $T = T_r$, (T_r is the room temperature) by transistor size ratio, which is given by

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\frac{\mu_n(T_0)}{\mu_p(T_0)}\left(\frac{T_r}{T_0}\right)^{m_p-m_n}}{\left(\frac{\alpha_{VTp}}{\alpha_{VTn}}\right)^2\left(\frac{1}{2}+\frac{m_n}{2m_p}\right)^2}. \tag{4.37}$$

The minimum required power supply should be considered at the lowest operating temperature, $T_{\min}$, where V_{THn} and $|V_{THp}|$ are maximum, and it is given by

$$V_{DDmin} = \left(\frac{R_1}{R_2}+1\right)V_{GSn}(T_{\min}) + |V_{DS5(sat)}| \tag{4.38}$$

which shows that the circuit is able to operate with low-power supply voltage when low-threshold voltage devices are available.

The experimental results in [46] show an average temperature drift of 36.9 ppm/°C over the temperature range of 0°C-100°C. This circuit is reproducible in any CMOS technology.

4.2.3 CMOS Voltage Reference Based on the Mutual Compensation of Mobility and Threshold Voltage

As it was discussed earlier for a MOS transistor, the mobility and the threshold voltage are the two parameters that have a strong temperature dependence. It was also shown that mutual compensation of the mobility and the threshold voltage results in a temperature stable bias point of a MOS transistor. This effect has been used for the design of CMOS voltage references [47], [48]. The circuit proposed in [48], is similar to the voltage references using Zener diodes and is shown in Figure 4.14. In this circuit, for transistor M_1

$$I_{D1} = V_{GS1}\frac{R_2}{R_1R_3}. \tag{4.39}$$

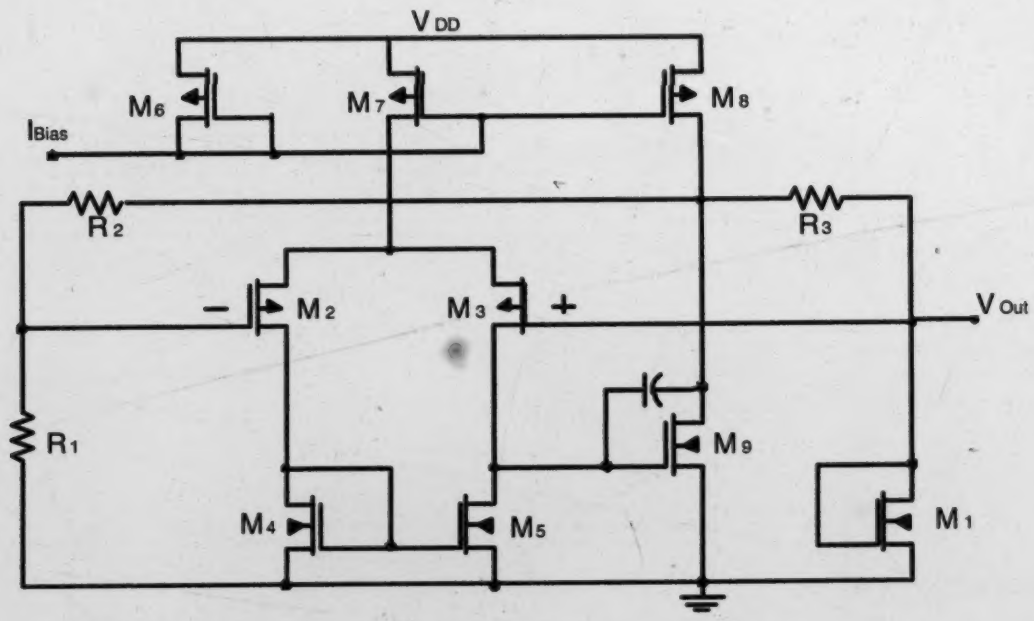


Figure 4.14: Schematic of the voltage reference using ZTC point (after [48])

One should choose the resistors R_1, R_2 and R_3 so that $I_{D1} = I_{DF}$ and $V_{GS1} = V_{GSF}$. Assuming that the temperature behavior of the resistors is described as $R_i = R_{i0}(1 + k_i\Delta T)$, (i=1,2,3), and using (4.39), the variation of I_{D1} due to the resistor temperature dependencies is obtained as

$$I_{D1} + \Delta I_{D1} = I_{DF} + \Delta I_{D1} \approx V_{GSF}\frac{R_{20}}{R_{10}R_{30}}[1 + (k_2 - k_1 - k_3)\Delta T]. \qquad (4.40)$$

This variation becomes zero when $k_2 = k_1 + k_3$. This circuit was implemented in 0.35-μm technology. The polysilicon resistor is used for the realization of resistor R_1 and R_3 and R_2 were implemented using n^+-diffusion layer. Experimental results show an average temperature drift of 10 ppm/°C.

4.3 Conclusion

Voltage references are essential building blocks of many analog and digital circuits. The bandgap references is the most popular voltage reference used in circuit design. This reference provides an output voltage with low sensitivity to the temperature and process variations. Bandgap references are bipolar in nature but can be implemented in CMOS technology as well by replacing the BJT transistors with parasitic vertical bipolar junction transistor formed in a p-well or n-well. In this chapter, the basic principles behind the design of bandgap reference were discussed. The techniques used to improve the temperature-behavior of a bandgap reference output voltage, such as quadratic temperature compensation, second-order curvature-compensated reference using resistor ratio and piecewise-linear curvature correction, as well as methods for the design of low-voltage BGR were studied. Finally, we presented the techniques used for the implementation of CMOS non-bandgap voltage references with the performance comparable to the performance of BGR.

Chapter 5

New non-Bandgap CMOS Voltage References

In Chapter 4, we reviewed several techniques used in the design of voltage references. It was mentioned that the bandgap reference is the most widely used reference since its output voltage is stable against temperature and process variations. However, when the power supply is below 1 V, the performance of a conventional bandgap reference degrades. A number of methods which have been used for the design of low-voltage bandgap references were introduced, but these techniques required non-standard devices or complex circuits. It was also mentioned that the presence of ZTC point in the transconductance characteristics of a MOS transistor has been used for the design of CMOS voltage references. However, for low voltage design the power supply might be lower than the ZTC point.

In this chapter, we first propose a voltage reference using transistors with a ZTC point, biased with constant currents. Then, the temperature behavior of the gate-source voltage of a CMOS transistor biased with a PTAT current source will be investigated. This will be followed by designing two CMOS voltage references in 0.18-μm technology using transistors biased with PTAT currents.

5.1 Generation of a Virtual ZTC point

It was shown in Chapter 2 that the transconductance characteristics of a MOS transistor at different temperatures will have a common intercept point called the ZTC point. It was shown analytically that this point exists when the mobility parameter, m, is equal to 2 [14]. However, the value of m dependens on many factors, one of which is the dopant concentration. Consequently, m might not be equal to 2 and in such cases the transconductance characteristics has a bottleneck and an exact point of temperature compensation does not exist. To show this, a single NMOS transistor was simulated in 0.18-μm technology and the resulting transconductance characteristics are shown in Figure 5.1. One can see clearly from Figure 5.1(b) that an exact point of temperature compensation does not exist.

This figure also shows that when the transistor is biased with a constant current, I_D, above the ZTC point vicinity, the gate-source voltage has a positive temperature dependency and when it is biased with a temperature-stable constant current below the ZTC point vicinity, the gate-source voltage has a negative temperature dependency.

The idea of a virtual ZTC point is that by summing the gate-source voltages of two diode-connected transistors, biased by temperature-stable constant currents, one below the ZTC vicinity and another above the ZTC vicinity, one can obtain a temperature independent voltage.

To explain the idea theoretically, the temperature coefficient of the gate-source voltage of a MOS transistor biased with a constant current should be derived.

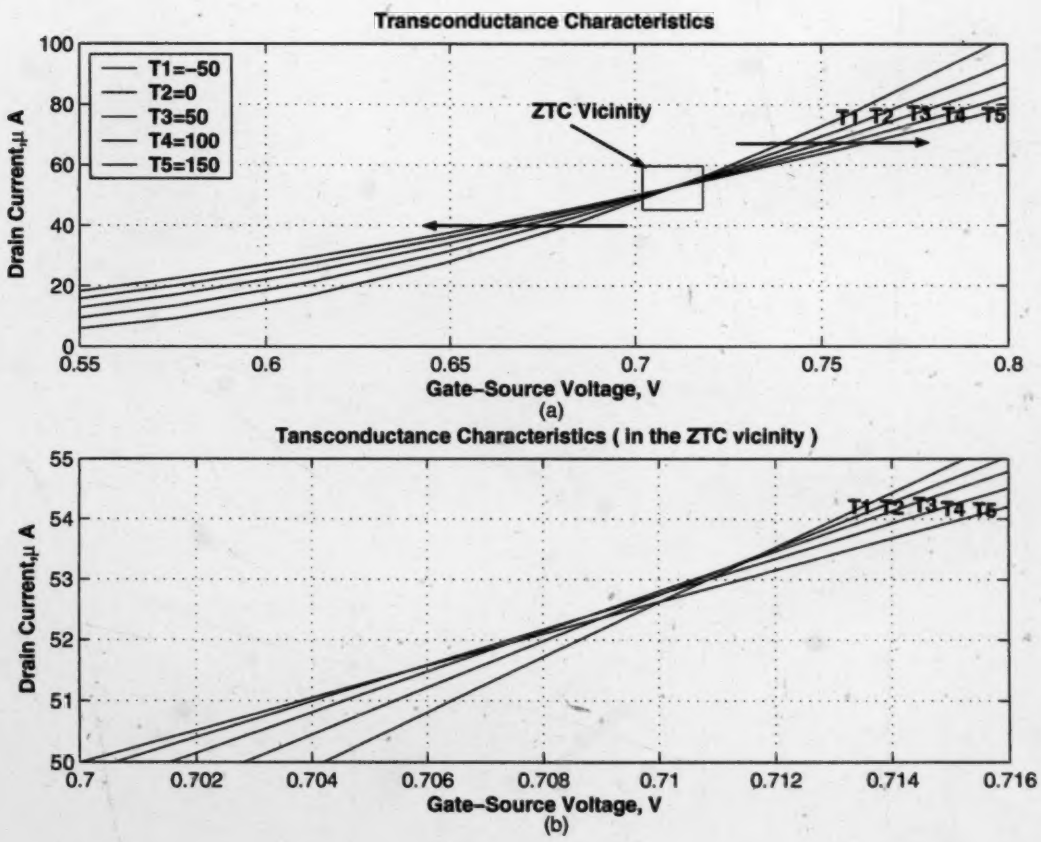


Figure 5.1: Simulated transconductance characteristics of an NMOS transistor

Let a diode-connected transistor be biased with a constant current I_D. The gate-source voltage of such a transistor is given by [20]

$$V_{GS}(T) = V_{TH}(T) + K'\sqrt{I_D/\mu(T)} \tag{5.1}$$

where $K' = \sqrt{\frac{2}{C_{ox}(\frac{W}{L})}}$. The temperature dependency of the threshold voltage and the mobility were given in (2.7) and (2.17), respectively and will be repeated here for convenience. The threshold voltage depends on the temperature as

$$V_{TH}(T) = V_{TH0} - \alpha_{VT}(T - T_0) \tag{5.2}$$

where V_{TH0} is the threshold voltage at $T = T_0$ and α_{VT} is a positive constant. The temperature dependency of the mobility is given by

$$\mu(T) = \mu_0 \left(\frac{T}{T_0}\right)^{-m} \tag{5.3}$$

where m is a positive constant. Substituting (5.2) and (5.3) into (5.1), the gate-source voltage can be written as

$$V_{GS}(T) = V_{TH0} - \alpha_{VT}(T - T_0) + K(\frac{T}{T_0})^{\frac{m}{2}}\sqrt{I_D} \tag{5.4}$$

where $K = K'/\sqrt{\mu_0}$. In order to find the temperature coefficient of the gate-source voltage we increase the temperature from T_0 to $T_0 + \delta T$, where δT is small, and we find the change of the gate-source voltage. Using (5.4), the gate-source voltage at $T = T_0$ is equal to

$$V_{GS}(T_0) = V_{TH0} + K\sqrt{I_D}. \tag{5.5}$$

When the temperature is increased to $T_0 + \delta T$, the gate-source voltage is equal to

$$V_{GS}(T_0 + \delta T) = V_{TH0} - \alpha_{VT}\delta T + K(1 + \frac{\delta T}{T_0})^{\frac{m}{2}}\sqrt{I_D}. \tag{5.6}$$

Subtracting (5.5) from (5.6), we find the change in the gate-source voltage with temperature as

$$\begin{aligned} \delta V_{GS} =& V_{GS}(T_0 + \delta T) - V_{GS}(T_0) \\ =& -\alpha_{VT}\delta T + \lambda[(1 + \frac{\delta T}{T_0})^{\frac{m}{2}} - 1] \end{aligned} \tag{5.7}$$

where $\lambda = K\sqrt{I_D}$. The Taylor series of $(1 + \frac{\delta T}{T_0})^{\frac{m}{2}}$ is found to be

$$(1 + \frac{\delta T}{T_0})^{\frac{m}{2}} = 1 + \frac{1}{2}\frac{m}{T_0}\delta T + \frac{1}{4}\frac{m(0.5m-1)}{T_0^2}\delta T^2 + O(\delta T^3). \tag{5.8}$$

Since δT is small, the high-order terms in (5.8) can be neglected. Therefore, equation (5.8) can be simplified to

$$(1 + \frac{\delta T}{T_0})^{\frac{m}{2}} \cong 1 + \frac{m}{2}\frac{\delta T}{T_0}. \tag{5.9}$$

Substituting (5.9) in (5.7), the temperature coefficient of the gate-source voltage to the first-order approximation is obtained as

$$\frac{\delta V_{GS}}{\delta T} \cong (-\alpha_{VT} + \frac{\lambda}{2}\frac{m}{T_0}). \tag{5.10}$$

Equation (5.10) shows that the temperature dependence of the gate-source voltage of a MOS transistor biased by a constant current can be controlled by parameter λ, i.e., the value of the bias current. The gate-source voltage will be temperature-independent if the bias current is set to

$$I_{DZ} = I_D = [\frac{2T_0\alpha_{VT}}{Km}]^2 = \frac{2T_0^2\alpha_{VT}^2}{m}\mu_0 C_{ox}(\frac{W}{L}). \tag{5.11}$$

If $m = 2$, then equation (5.11) will give the ZTC point current I_{DF}, defined in equation (2.23). When the current I_D is larger than I_{DZ}, the temperature coefficient of the gate-source voltage is positive, and when I_D is smaller than I_{DZ}, the temperature coefficient of the gate-source voltage is negative.

5.1.1 Circuit Design and Analysis

To verify that a virtual ZTC point can be generated, we designed a circuit consisting of two NMOS diode-connected transistors, one biased with a constant current below the ZTC vicinity and another above the ZTC vicinity. The circuit is shown in Figure 5.2 and the value of the resistor, R_B, and the sizes of the transistors are given in Table 5.1. Transistors $(M_1 - M_4)$ and resistor R_B form the current source which is based on the architecture shown in Figure 3.3. All the transistors are operating in the saturation region. The circuit is designed in such a way that the diode-connected transistor M_7 is biased with a current I_7 which is less than I_{DF} and transistor M_8 is biased with I_8, which is larger than I_{DF}. Using KVL, for the loop consisting of transistors $(M_3 - M_4)$ and Resistor R_B, one can write

$$R_B I_B = V_{SG4} - V_{SG3} = \sqrt{\frac{I_B K_4'}{\mu(T)}} - \sqrt{\frac{I_B K_3'}{\mu(T)}}, \tag{5.12}$$

where $K' = \sqrt{\frac{2}{C_{ox}(\frac{W}{L})}}, i = 3, 4$. Solving (5.12) for I_B we obtain

$$I_B = \frac{2}{\mu(T) C_{ox} R_B^2} \left(\frac{1}{\sqrt{(W/L)_4}} - \frac{1}{\sqrt{(W/L)_3}} \right)^2. \tag{5.13}$$

The temperature dependence of the resistor is given by

$$R_B = R_0(1 + \alpha_{R1}(T - T_0) + \alpha_{R2}(T - T_0)^2) \tag{5.14}$$

where α_{R1} and α_{R2} are the first and second-order temperature coefficients of the resistor. Substituting (2.17) for the temperature dependence of the mobility and equation (5.14) for the temperature dependency of R_B in (5.13), the Taylor series expansion of equation (5.13) will be equal to

$$I_B = \left(\frac{I_{B0}}{R_0}^2 \right) \{1 + (\frac{m}{T_0} - 2\alpha_{R1})(T - T_0) + \left(-2\alpha_{R2} + 3\alpha_{R1}^2 + \frac{m(m-1)}{2T_0^2} + \frac{m^2}{T_0^2} - \frac{2m\alpha_{R1}}{T_0} \right) (T - T_0)^2\} + O((T - T_0)^3) \tag{5.15}$$

Table 5.1: Transistor and resistor sizes for the circuit shown in Figure 5.2

M_{s1}	M_{s2}	M_{s3}	M_1	M_2	M_3	M_4
$\frac{3\mu}{2\mu}$	$\frac{0.42\mu}{2\mu}$	$\frac{3\mu}{2\mu}$	$\frac{15\mu}{2\mu}$	$\frac{11\mu}{2\mu}$	$\frac{7\mu}{2\mu}$	$\frac{7\mu}{2\mu}$
M_5	M_6	M_7	M_8	R_B	R_1	R_2
$\frac{11\mu}{2\mu}$	$\frac{16.2\mu}{2\mu}$	$\frac{8\mu}{2\mu}$	$\frac{8\mu}{2\mu}$	$2k\Omega$	$20k\Omega$	$20k\Omega$

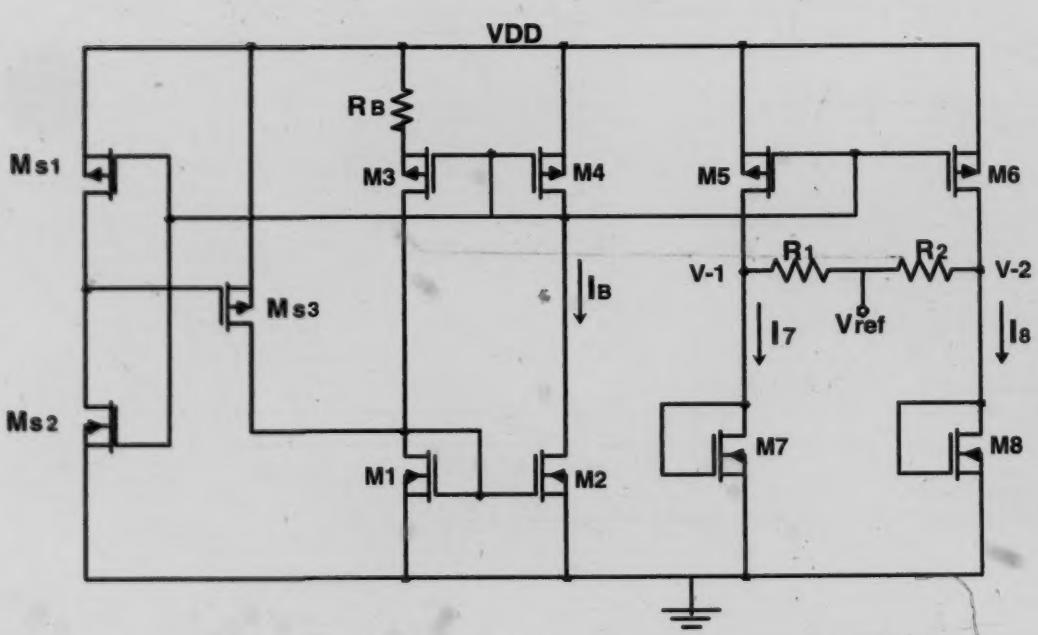


Figure 5.2: Voltage reference using constant bias currents

where $I_{B0} = \frac{2}{C_{ox}\mu_0 R_0^2}\left(\frac{1}{\sqrt{(W/L)_4}} - \frac{1}{\sqrt{(W/L)_3}}\right)^2$ and T_0 is the reference temperature. Consequently, to a first-order approximation, the current I_B can be written as

$$I_B \simeq I_{B0}(1+\gamma(T-T_0)) \tag{5.16}$$

where $\gamma = (\frac{m}{T_0} - 2\alpha_{R1})$. Hence, the current source will generate a temperature-independent (TI) current when

$$\alpha_{R1} = \frac{m}{2T_0}. \tag{5.17}$$

Transistors M_5 and M_6 mirror the current I_B and supply TI currents to the transistors M_7 and M_8.

The output voltage in the circuit shown in Figure 5.2 is given by

$$V_{ref} = \frac{V_{GS7}}{1+(R_1/R_2)} + \frac{V_{GS8}}{1+(R_2/R_1)}. \tag{5.18}$$

Since the output voltage depends on the ratio of resistors R_1 and R_2, the sensitivity of the output voltage to the variations of R_1 and R_2 is reduced. We assumed that R_1=R_2. All the resistors are realized using an N^+ nonsilicide diffusion layer with $\alpha_{R1} = 1.47 \times 10^{-3}\text{deg}^{-1}$ and $\alpha_{R2} = 0.832 \times 10^{-6}\text{deg}^{-2}$. By taking the derivative of (5.18) with respect to the temperature, we can find that the temperature coefficient of the reference voltage is

$$\begin{aligned}\frac{\delta V_{ref}}{\delta T} &= 0.5\left(\frac{\delta V_{GS7}}{\delta T} + \frac{\delta V_{GS8}}{\delta T}\right) \\ &= -2\alpha_{VT} + \frac{m}{2T_0}(\lambda_7+\lambda_8)\end{aligned} \tag{5.19}$$

where $\lambda_7 = K_7\sqrt{\frac{(W/L)_5}{(W/L)_4}I_{B0}}$, $\lambda_8 = K_8\sqrt{\frac{(W/L)_6}{(W/L)_4}I_{B0}}$ and $K_i = K_i'/\sqrt{\mu_0}(i=7,8)$. Transistors M_7 and M_8 have the same length and width, and therefore, $K_7 = K_8$. Using (5.19), if the sizes of transistors M_5 and M_6 are chosen to satisfy

$$\sqrt{\left(\frac{W}{L}\right)_5} + \sqrt{\left(\frac{W}{L}\right)_6} = \frac{4T_0\alpha_{VT}}{mK_7\sqrt{I_{B0}}}\sqrt{(\frac{W}{L})_4} \tag{5.20}$$

then the reference voltage will be temperature-independent.

5.1.2 Simulation Results

The circuit in Figure 5.2 was simulated over the temperature range $-50°C$ to $150°C$ using a power supply voltage of 1.8 V. Figure 5.3 shows the simulation results for the currents, I_B, I_7 and I_8. As it can be seen, the changes of the currents, I_B, I_7 and I_8 over the temperature range -50°C-150°C are less than $3\mu A$.

Figure 5.4 shows the simulation results for the gate-source voltages of transistors M_7, M_8 and the output voltage V_{ref}. The change in the output voltage, obtained in simulation, is 4mV over the temperature range of $-50°C$ to $150°C$ and its temperature stability is equal to 28 ppm/°C. Since the temperature-dependence of the bias current is not exactly zero, a nonlinear temperature-dependent error voltage appears at the reference output voltage. The results of simulation verify that the circuit operates according to the analysis given above and a temperature-stable voltage can be obtained.

Equation (5.12), has an additional solution, and that is $I_B = 0$. If the current source falls into this state, the generated current will be zero and the circuit will not work. Therefore, a start-up circuit is required to prevent the circuit from remaining in the zero-current state. A start-up circuit ensures a non-zero current state by flowing a small amount of current to the current generator. An additional requirement is that the start-up circuit must not interfere with the normal operation of the reference once the desired operating point is reached. In Figure 5.2, transistors $(M_{s1} - M_{s3})$ form the start-up circuit which operates as follows. When the gate voltage of M_3 is high, transistor M_{s2} turns on and pulls down the gate voltage of transistor M_{s3}. This causes transistor M_{s3} to turn on and pull up the gate-drain connection of transistor M_1. As a result, transistors $(M_1 - M_3)$ will turn on and the current reference will be out of its zero-state mode. Consequently, the gate-voltage of transistor M_4 drops,

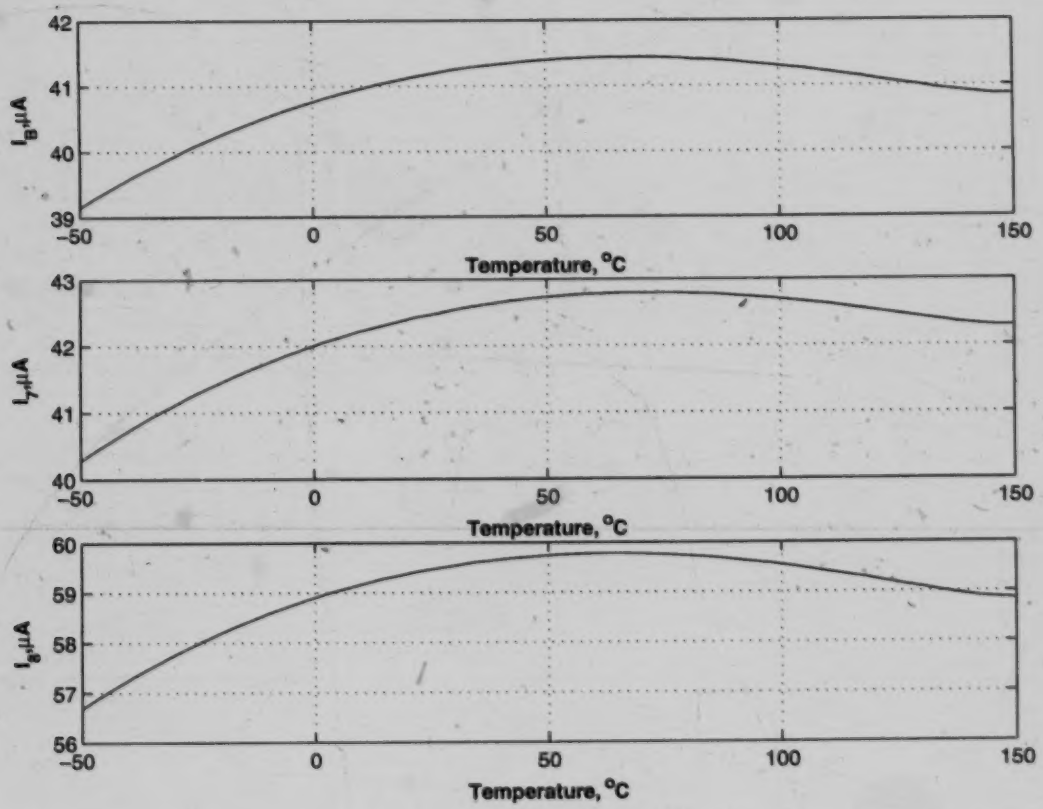


Figure 5.3: Simulation results for I_B, I_7 and I_8 for the circuit shown in Figure 5.2

transistor M_{s1} turns on, pulling up the gate voltage of transistor M_{s3} and turning it off.

To verify the performance of the start-up circuit, we replaced the power supply by a step voltage and performed a transient simulation. The waveforms are shown in Figure 5.5 and confirm the correct operation of the start-up circuit.

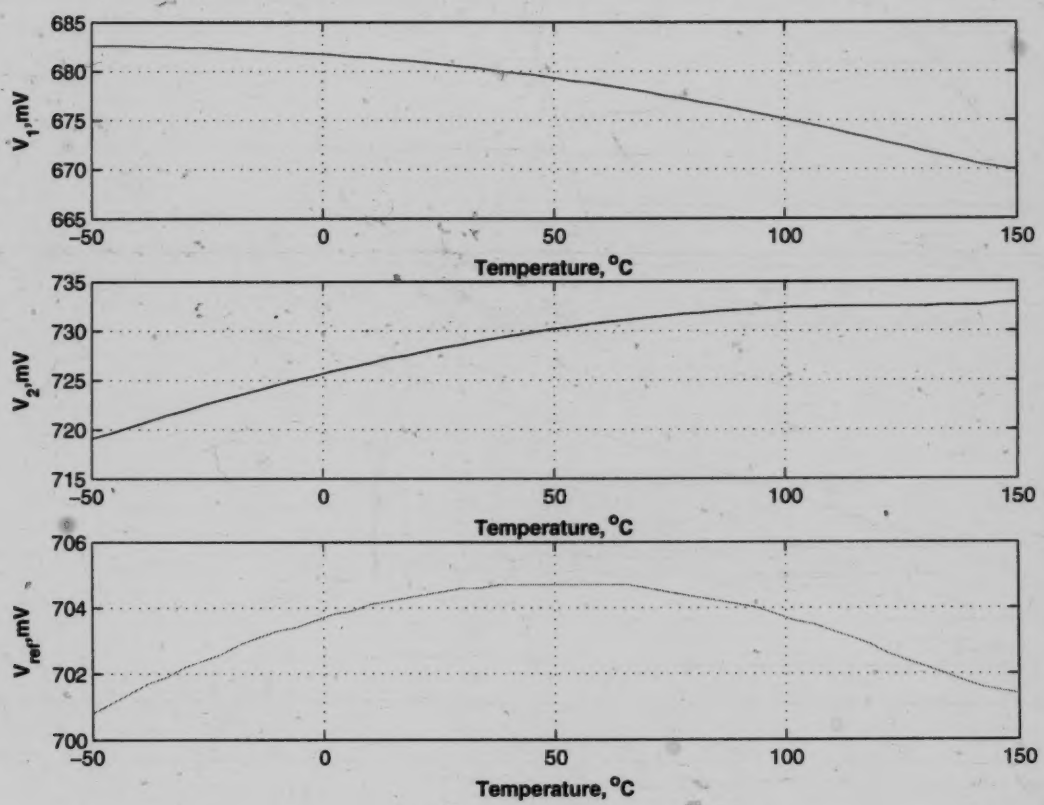


Figure 5.4: Simulation results for V_{GS7}, V_{GS8} and V_{ref} for the circuit shown in Figure 5.2

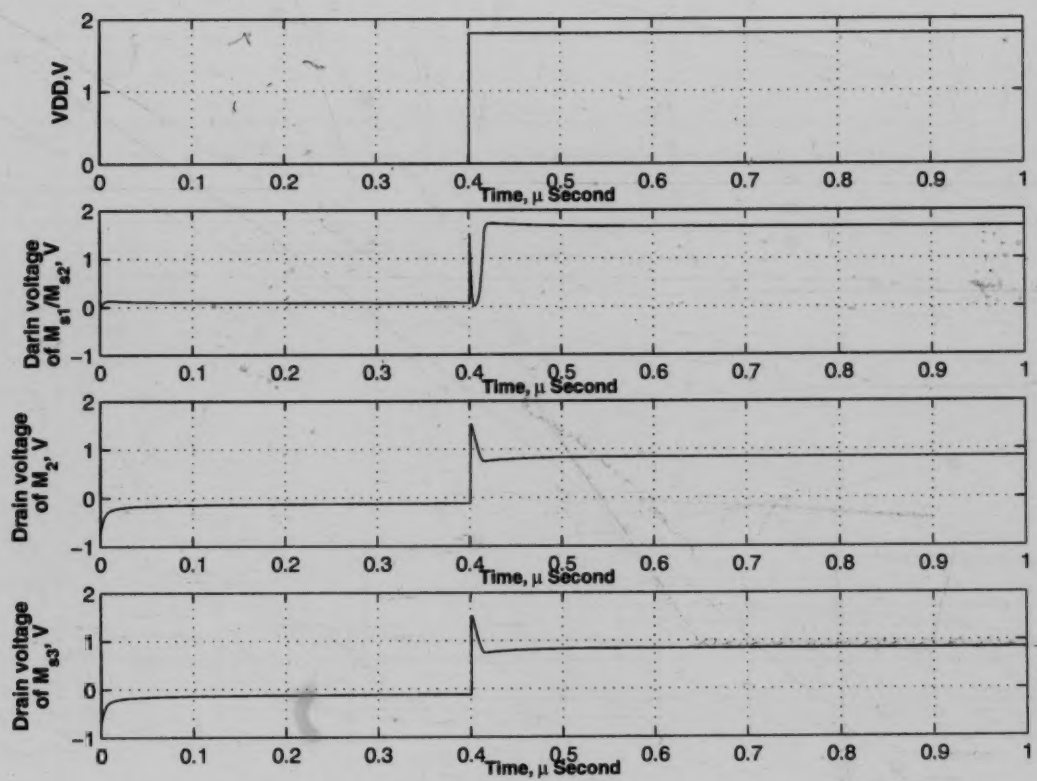


Figure 5.5: Simulation results for the start-up circuit in Figure 5.2

5.2 Diode-Connected Operation with PTAT Drain Current

In this section, we investigate the temperature behavior of the gate-source voltage of a MOS transistor when its drain current is proportional to the absolute temperature. Let us consider a diode-connected n-channel transistor biased by an external PTAT current, $I_D(T)$, which is expressed by

$$I_D(T) = I_{D0}[1 + \gamma(T - T_0)] \tag{5.21}$$

where γ is a positive constant and T_0 is the reference temperature. The gate-source voltage, V_{GS}, is equal to [20]

$$V_{GS}(T) = V_{TH}(T) + K'\sqrt{I_D(T)/\mu(T)} \tag{5.22}$$

where $K' = \sqrt{\frac{2}{C_{ox}(\frac{W}{L})}}$. The temperature behavior of the threshold voltage and the mobility were given in (5.2) and (5.3), respectively. Substituting (5.2) and (5.3) into (5.22), the gate-source voltage can be written as

$$V_{GS}(T) = V_{TH0} - \alpha_{VT}(T - T_0) + K(\frac{T}{T_0})^{\frac{m}{2}}\sqrt{I_D(T)} \tag{5.23}$$

where $K = K'/\sqrt{\mu_0}$. In order to find the temperature coefficient of the gate-source voltage, we increase the temperature from T_0 by a small amount of δT to $T_0 + \delta T$ and we find the change of the gate-source voltage. Using (5.23), at $T = T_0$ the gate-source voltage is equal to

$$V_{GS}(T_0) = V_{TH0} + K\sqrt{I_D(T_0)}. \tag{5.24}$$

When the temperature is increased to $T_0 + \delta T$, the gate-source voltage is equal to

$$V_{GS}(T_0 + \delta T) = V_{TH0} - \alpha_{VT}\delta T + K(1 + \frac{\delta T}{T_0})^{\frac{m}{2}}\sqrt{I_{D0}(1 + \gamma\delta T)}. \tag{5.25}$$

Subtracting (5.24) from (5.25), we find the change in the gate-source voltage with temperature to be

$$\begin{aligned}\delta V_{GS} &= V_{GS}(T_0+\delta T) - V_{GS}(T_0) \\ &= -\alpha_{VT}\delta T + \lambda[\sqrt{(1+\gamma\delta T)}(1+\frac{\delta T}{T_0})^{\frac{m}{2}} - 1]\end{aligned} \tag{5.26}$$

where $\lambda = K\sqrt{I_{D0}}$. The Taylor series expansion of $(1+\frac{\delta T}{T_0})^{\frac{m}{2}}$ is given in (5.8) and the Taylor series expansion of $\sqrt{(1+\gamma\delta T)}$ is found to be

$$\sqrt{(1+\gamma\delta T)} = 1 + \frac{1}{2}\gamma\delta T - \frac{1}{8}\gamma^2\delta T^2 + O(\delta T^3). \tag{5.27}$$

Since δT is small, the high-order terms in (5.27) can be neglected. Therefore, equation (5.27) can be simplified to

$$\sqrt{(1+\gamma\delta_T)} \cong 1 + \frac{\gamma\delta T}{2}. \tag{5.28}$$

Substituting (5.28) and (5.9) in (5.26), the temperature coefficient of the gate-source voltage, to a first-order approximation, is obtained as

$$\frac{\delta V_{GS}}{\delta T} \cong (-\alpha_{VT} + \frac{\lambda}{2}(\frac{m}{T_0} + \gamma)). \tag{5.29}$$

Equation (5.29) shows that the variables which can be used by the designer to alter the temperature behavior of V_{GS} for a specific transistor are I_{D0} and γ which are, in fact, parameters of the current source. Overall, these parameters can be chosen to make the temperature coefficient of the gate-source voltage of such a transistor, positive, negative or zero. Figures 5.6 and 5.7 show the simulated transconductance characteristics (with a temperature as a parameter) for a typical NMOS transistor in 0.18-μm CMOS technology. Figure 5.6 shows the case for which the parameters of the current source are chosen to make $V_{GS}(T)$ temperature independent. Figure 5.7 shows the cases for which the PTAT current parameters are chosen to make the temperature dependence of V_{GS} positive and negative.

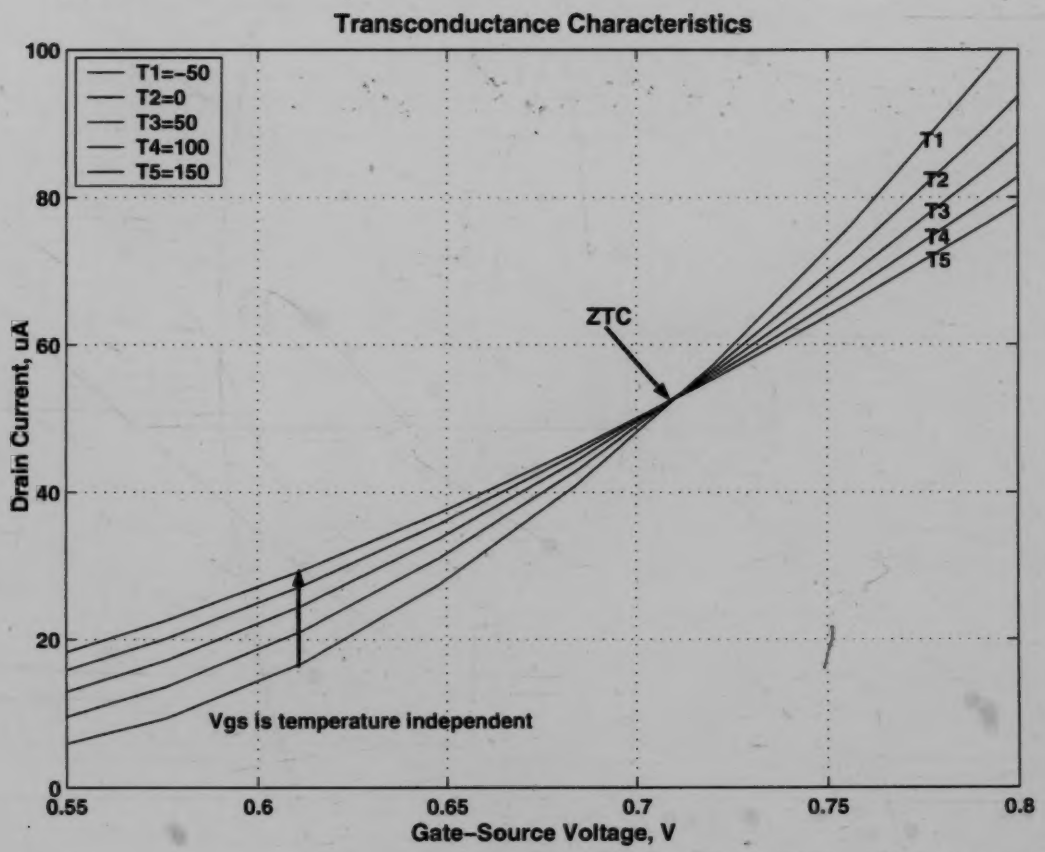


Figure 5.6: Simulated transconductance characteristics of an NMOS transistor

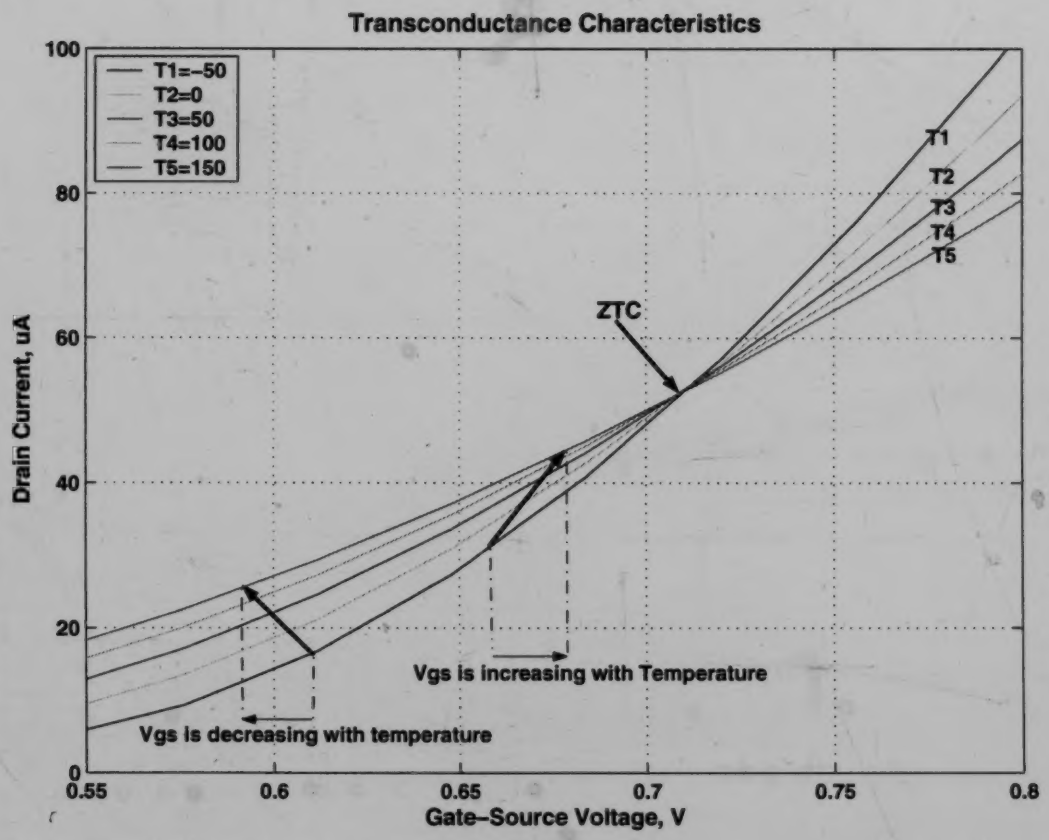


Figure 5.7: Simulated transconductance characteristics of an NMOS transistor

5.3 A Simple Voltage Reference Using a PTAT Current Source

It was shown in the previous section that the designer can alter the temperature coefficient of the gate-source voltage of a diode-connected transistor biased with a PTAT current, by changing the PTAT current source parameters. Therefore, according to (5.29), in order to have a temperature-independent V_{GS} for a diode-connected transistor biased with a PTAT current, the current parameters λ and γ should satisfy

$$\frac{\lambda}{2}(\frac{m}{T_0}+\gamma) = \alpha_{VT}. \tag{5.30}$$

This condition can be used to design a simple CMOS voltage reference, as explained in the next section.

5.3.1 Circuit Design and Analysis

A circuit consisting of a PTAT current reference and a diode-connected NMOS transistor is designed in 0.18-μm TSMC technology. The circuit is shown in Figure 5.8. The value of the resistor, R_B, and the sizes of the transistors are given in Table 5.2. Transistors ($M_1 - M_4$) and Resistor R_B form the current reference circuit. The current reference circuit is similar to the current reference used in Figure 5.2. The only difference is that the current in the circuit shown in Figure 5.8 is generated by the gate-source voltage difference of two NMOS transistors, while in the circuit shown in Figure 5.2, the current is generated by the gate-source voltage difference of two PMOS transistors. The operation is similar and both current references generate a current which is given by

$$I_B = I_{B0}(1+\gamma(T-T_0)) \tag{5.31}$$

where

$$\gamma = \frac{m}{T_0} - 2\alpha_{R1}. \tag{5.32}$$

Note that in the Figure 5.2 a constant current was required, i.e., $\gamma \simeq 0$, while in the circuit shown in Figure 5.8 a PTAT current is required, i.e., $\gamma > 0$. In (5.32), m is in the range of (1.5-2) for the electron mobility and assuming $T_0 = 27°C$, α_{R1} should be less than $0.0278/°C$ in order to have $\gamma > 0$. We used N^+ non-silicide diffusion with $\alpha_{R1} = 1.47 \times 10^{-3}\text{deg}^{-1}$ and $\alpha_{R2} = 0.832 \times 10^{-6}\text{deg}^{-2}$ for the realization of the resistor.

In Figure 5.8, transistors ($M_{s1} - M_{s3}$) form the start-up circuit. The structure is different from the one used in Figure 5.2. When the power supply is turned on, M_{s1} is initially on and operates in the triode region and transistor M_{s2} is off. The voltage at the gate of M_{s3} is high and therefore, its drain is down, pulling the gate of M_2 down as well. As soon as the gate-drain voltage of transistor M_4 increases, the drain voltage of transistor M_{s2} decreases, which turns off transistor M_{s3}.

In Figure 5.8, transistor M_5 mirrors the current I_B by a factor of $\frac{(W/L)_5}{(W/L)_1}$. As a result, the current that biases transistor M_6 is given by

$$I_{D6} = I_{D60}[1 + \gamma(T - T_0)] \tag{5.33}$$

where $I_{D60} = \frac{(W/L)_5}{(W/L)_1} I_{B0}$ and γ is given by (5.32). To obtain a temperature-independent V_{GS6}, the parameters of the current I_{D6} should satisfy (5.30), where $\lambda = K_6\sqrt{I_{D60}}$. Using (5.32), (5.30) and (5.33), the design equation is obtained as

$$\sqrt{\frac{(\frac{W}{L})_5}{(\frac{W}{L})_1}} = \frac{\alpha_{VT}}{K_6\sqrt{I_{B0}}(\frac{m}{T_0} - \alpha_{R1})}. \tag{5.34}$$

Therefore, if the sizes of transistors M_1 and M_5 satisfy (5.34), the gate-source voltage, V_{GS6}, will be temperature-independent.

Table 5.2: Transistor and resistor sizes for the circuit shown in Figure 5.8

M_{s1}	M_{s2}	M_{s3}	M_1	M_2
$\frac{.42\mu}{2\mu}$	$\frac{10\mu}{2\mu}$	$\frac{3\mu}{2\mu}$	$\frac{8\mu}{2\mu}$	$\frac{8\mu}{2\mu}$
M_3	M_4	M_5	M_6	R_B
$\frac{5.5\mu}{2\mu}$	$\frac{4\mu}{2\mu}$	$\frac{18.4\mu}{2\mu}$	$\frac{8\mu}{2\mu}$	$2k\Omega$

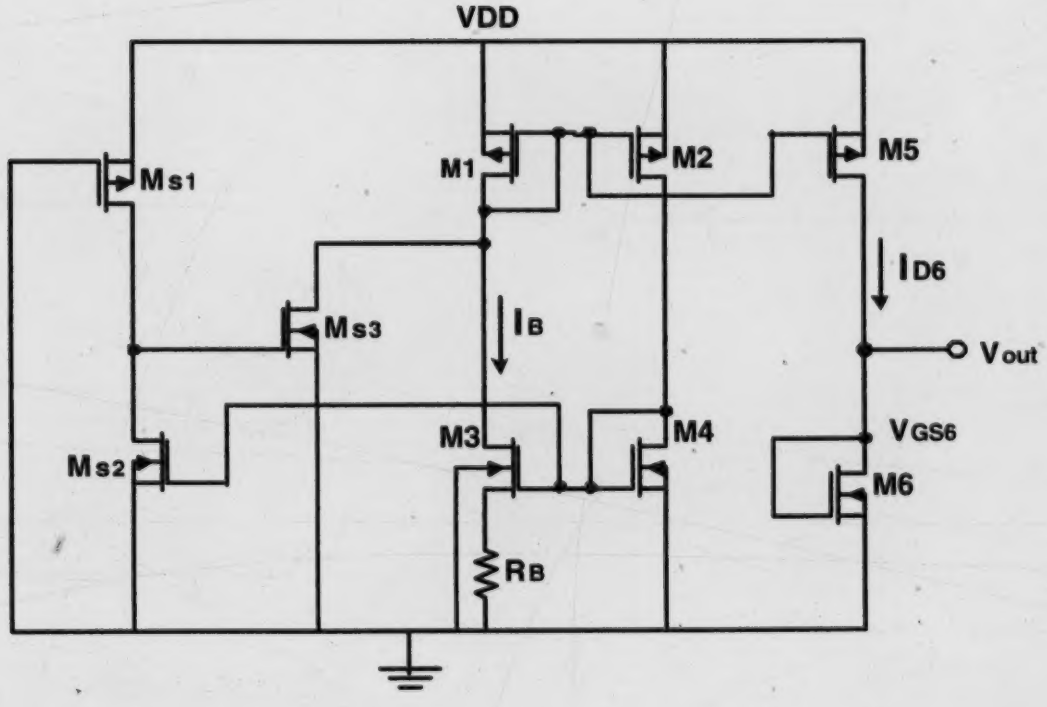


Figure 5.8: Voltage reference using a diode-connected transistor biased with a PTAT current source

The above analysis is based on the assumption that all the MOS transistors are operating in the saturation region. Thus the minimum supply voltage must be maintained in order to prevent the current source M_5 from being forced to operate in the triode region. Since V_{THn} and $|V_{THp}|$ have negative temperature coefficients, the minimum required power supply should be evaluated at the lowest operating temperature. That is,

$$V_{DDmin} = (V_{THn})_{\max} + |V_{DS5}(sat)|. \tag{5.35}$$

Note that the circuit can be easily designed with the saturation voltage, $|V_{DS5}(sat)|$ less than 0.2 V and therefore, the minimum required power supply can be less than 1 V.

5.3.2 Simulation Results

The circuit shown in Figure 5.8 was simulated in the temperature range of $-50°C$ to $150°C$ using a power supply voltage of 1.8 V. Figure 5.9 shows the simulation results for the PTAT currents, I_B and I_6 and the gate-source voltage V_{GS6}. Note that currents I_B and I_6 increase as the temperature increases and they can be approximated as a linear function of temperature with the temperature coefficient of $\gamma = 1.85 \times 10^{-3}/°C$. However, as (5.15) shows, I_B includes higher-order temperature terms that results in not an exact linearalization of PTAT currents.

The change in the gate-source voltage of transistor M_6 is $500\mu V$ only, over the temperature range of $-50°C$ to $150°C$ and its temperature stability is equal to 4 ppm/°C. Since the temperature-dependency of the threshold voltage and bias current are not perfectly linear in the whole temperature range, a nonlinear residue appearing on the V_{GS6} waveform. The results of simulation verify that the circuit operates according to the analysis given above.

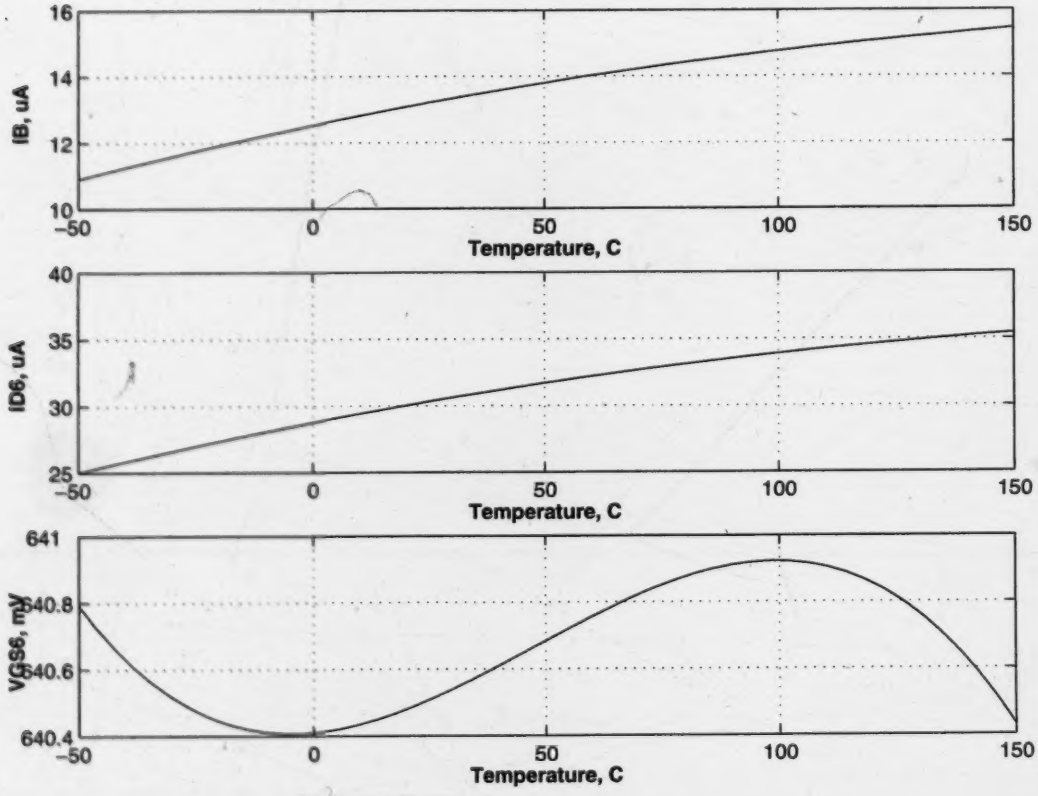


Figure 5.9: Simulation results for I_B, I_{D6} and V_{GS6} for the circuit shown in Figure 5.8

5.4 A Sub-1-V Voltage Reference

It was shown in Section 5.2 that it is possible to control the temperature coefficient of the gate-source voltage of a diode-connected transistor biased with a PTAT current by altering the parameters of the PTAT current source. Using this feature, we have designed a sub-1-V CMOS voltage reference, which takes advantage of summing the gate-source voltages of two NMOS transistors operating in the saturation region. Both transistors are working below their ZTC points. The PTAT currents are used to bias two diode-connected transistors in such a way that their drain voltages will have opposite temperature coefficients. Then, on a resistor connecting their drains, one can find a point where the voltage does not change with temperature. The voltage reference circuit is shown in Figure 5.10 and it is implemented in a standard 0.18-μm CMOS process. The values of the resistors and the sizes of the transistors are given in Table 5.3. The circuit consists of three parts: i) a start-up circuit (transistors M_{s1}-M_{s3}) which is the same as the one used in Section 5.3, ii) a PTAT current source (transistors M_1-M_4 and resistor R_B) similar to the one used in Section 5.3 and iii) the reference core circuit (two diode-connected transistors M_7 and M_8 operating below their ZTC points). Transistors M_5 and M_6 supply PTAT currents to the transistors M_7 and M_8. As it was shown in the previous sections, the PTAT current source generates the current

$$I_B(T) = I_{B0}[1 + \gamma(T - T_0)], \tag{5.36}$$

where $\gamma = \frac{m}{T_0} - 2\alpha_{R1}$. Again, we have used an N^+ nonsilicide diffusion layer with $\alpha_{R1} = 1.47 \times 10^{-3}\text{deg}^{-1}$ for the realization of the resistor, R_B.

Table 5.3: Transistor and resistor sizes for the circuit shown in Figure 5.10

M_{s1}	M_{s2}	M_{s3}	M_1	M_2	M_3	M_4
$\frac{.42\mu}{2\mu}$	$\frac{10\mu}{2\mu}$	$\frac{3\mu}{2\mu}$	$\frac{8\mu}{2\mu}$	$\frac{8\mu}{2\mu}$	$\frac{5.5\mu}{2\mu}$	$\frac{4\mu}{2\mu}$
M_5	M_6	M_7	M_8	R_B	R_1	R_2
$\frac{12.4\mu}{2\mu}$	$\frac{25\mu}{2\mu}$	$\frac{8\mu}{2\mu}$	$\frac{8\mu}{2\mu}$	$2k\Omega$	$20k\Omega$	$20k\Omega$

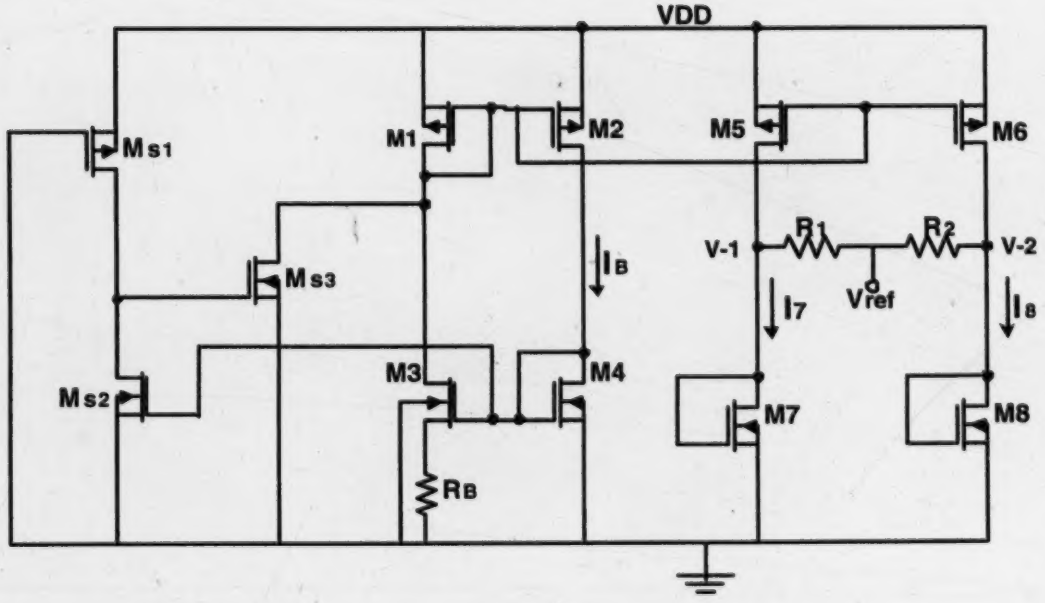


Figure 5.10: A Sub-1-V voltage reference

5.4.1 Circuit Design and Analysis

In Figure 5.10, the output voltage reference is given by

$$V_{ref} = \frac{V_{GS7}}{1+\frac{R_1}{R_2}} + \frac{V_{GS8}}{1+\frac{R_2}{R_1}}. \tag{5.37}$$

Note that the reference voltage depends on the ratio of the resistors R_1 and R_2 and, therefore, the sensitivity of the temperature coefficient of the output voltage to the variation of R_1 and R_2 ratio (due to doping gradient, non-optimized layout and high stress area of die) is reduced.

The temperature coefficient of the output voltage is obtained by taking the derivative of equation (5.37) with respect to the temperature. Doing so and using (5.29), the temperature coefficient of the output voltage will be equal to

$$\begin{aligned}\frac{\delta V_{ref}}{\delta T} =& \frac{1}{1+(R_1/R_2)}\left(\frac{\delta V_{GS7}}{\delta T}\right) + \frac{1}{1+(R_2/R_1)}\left(\frac{\delta V_{GS8}}{\delta T}\right) \\ =& -\alpha_{VT} + \left(\frac{\lambda_7}{1+(R_1/R_2)} + \frac{\lambda_8}{1+(R_2/R_1)}\right)\left(\frac{m}{2T_0}+\frac{\gamma}{2}\right)\end{aligned} \tag{5.38}$$

where $\lambda_7 = K_7\sqrt{\frac{(W/L)_5}{(W/L)_1}I_{B0}}$, $\lambda_8 = K_8\sqrt{\frac{(W/L)_6}{(W/L)_1}I_{B0}}$ and $\gamma = \frac{m}{T_0} - 2\alpha_{R1}$. If the sizes of transistors M_5 and M_6 are chosen to satisfy

$$\frac{\sqrt{\left(\frac{W}{L}\right)_5}}{1+(R_1/R_2)} + \frac{\sqrt{\left(\frac{W}{L}\right)_6}}{1+(R_2/R_1)} = \frac{\alpha_{VT}\sqrt{\left(\frac{W}{L}\right)_1}}{(\frac{m}{T_0}-\alpha_{R1})(K_7'\sqrt{I_{B0}})} \tag{5.39}$$

then the reference voltage will be temperature-independent. The minimum required power supply is given by

$$V_{DD_{\min}} = (V_{THn})_{\max} + |V_{DS5}(sat)| \tag{5.40}$$

and the circuit can be easily designed with $V_{DS}(sat)$ of less than 0.2 V.

5.4.2 Simulation Results

The circuit shown in Figure 5.10 was simulated in the temperature range of $-50°C$ to $150°C$ using a power-supply voltage of 1.8 V. Figure 5.11 shows the simulation

results for the PTAT currents, I_B, I_7 and I_7. As it can be seen, the currents I_B, I_6 and I_7 increase as the temperature increases and they can be approximated as a linear function of temperature with a temperature coefficient of $\gamma = 1.85 \times 10^{-3}/°C$. However, (5.15) includes higher-order terms that results in not an exact linearalization of the PTAT currents.

Figure 5.12 shows the simulation results for the gate-source voltages of transistors M_7 and M_8 and the output voltage V_{ref}. The change in the output voltage, obtained in simulation, is only 0.5mV, over the temperature range of $-50°C$ to $150°C$ and its temperature stability is 4 ppm/°C. Since the temperature-dependence of the threshold voltage and bias current are not perfectly linear over the whole temperature range, a nonlinear temperature-dependent error voltage appears at the reference output voltage. The results of simulation verify that the circuit operates according to the analysis given above.

Another important parameter which should be considered in the design of voltage references is called power supply rejection ratio (PSRR). It applies to the changes in the reference voltage that result from variations in the power supply [17]. Figure 5.13 shows the change of the output voltage, V_{ref}, while the power supply, V_{DD} changes from 0 V to 2 V. The circuit was designed for the supply 1.8 V. When the power supply deviates by $\pm 10\%$ from 1.8 V, the change in the output voltage is approximately $\pm$4mV. Although the change in the output voltage seems to be small but it can be improved using suitable circuit solutions. In this project, we intended to focus on temperature stabilization and no attempts were made to improve the PSRR factor.

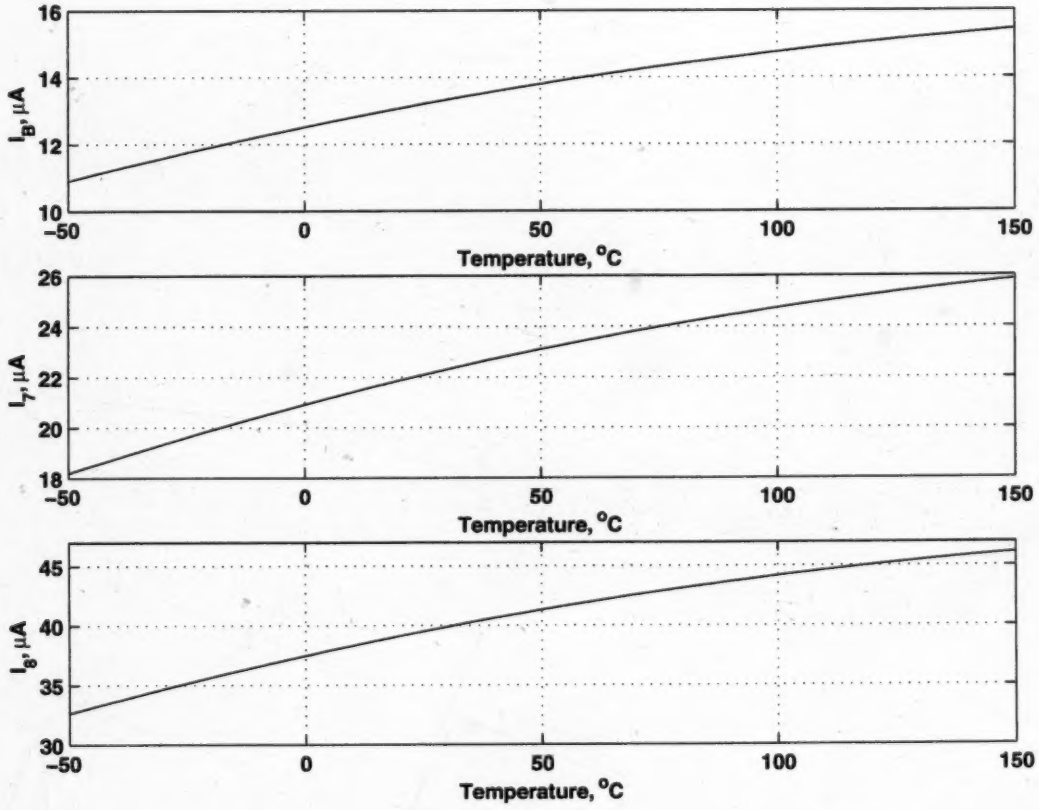


Figure 5.11: Temperature dependencies of I_B, I_7 and I_8 for the circuit shown in Figure 5.10

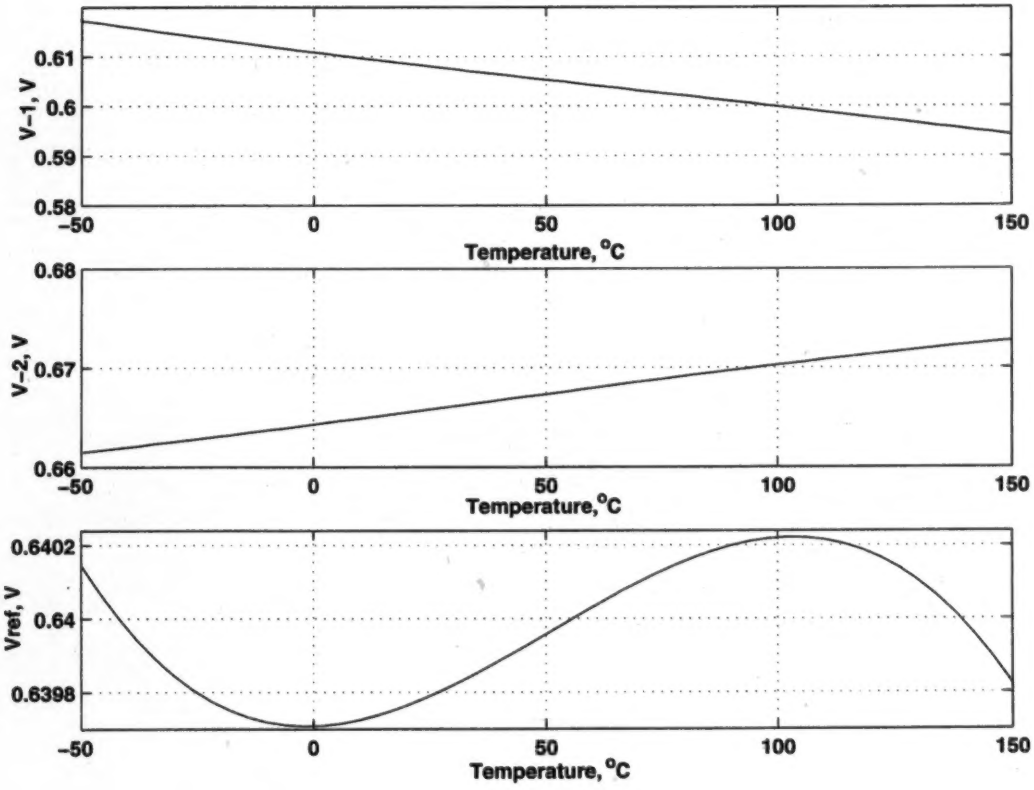


Figure 5.12: Temperature dependencies of V_{GS7}, V_{GS8} and V_{ref} for the circuit shown in Figure 5.10

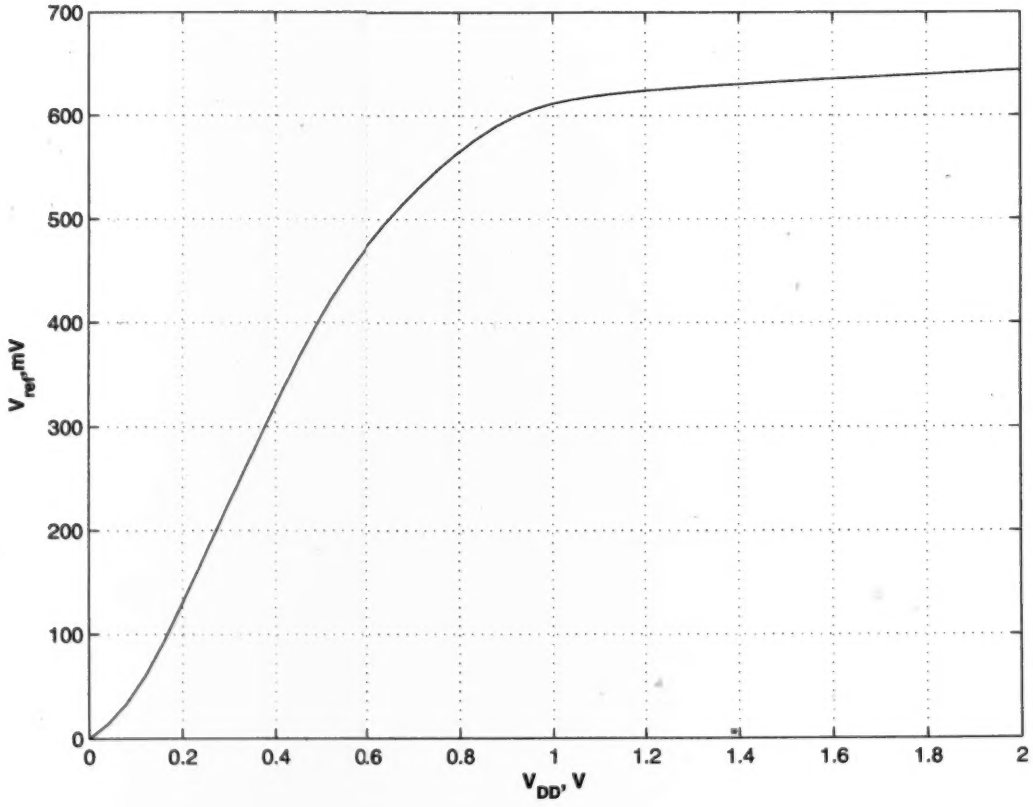


Figure 5.13: Change in V_{ref} due to the variation in power supply, for the circuit shown in Figure 5.10, $T = T_0 = 27°C$

5.5 Performance Comparison of Various Voltage References

A comparison of the voltage references proposed and studied in this thesis is tabulated in Table 5.4. For each design technique, the technology used to implement the voltage reference, the required power supply, V_{DD}, the output voltage, V_{ref} and the temperature coefficient of the reference voltage are given. Table 5.4 shows that the voltage references proposed in Section 5.3 and 5.4 have a much better temperature performance compared to the other non-bandgap references those of [44], [46] and [14]. Also one can see from Table 5.4 that the temperature performance of the circuits proposed in Sections 5.3 and 5.4 are comparable to the curvature compensated bandgap references of [3], [39] and [33]. The proposed references can be implemented in a standard CMOS technology unlike the voltage references of [44], which need extra fabrication steps for implementation. Also our voltage references can be designed for low voltage operation, while the voltage references [5] needs low threshold voltage devices for low voltage operation.

Table 5.4: Comparison of Various Voltage References

Design Technique	Technology	V_{DD}	V_{ref}	TC(ppm/°C)
First-order BGR using current processing [5]	0.4-μm CMOS	2.1 V	0.515 V	± 59(27°C-125°C)
Curvature-Compensated BGR using V_{PTAT}^2 [3]	6-μm CMOS	-	1.192 V	25.6 (-55°C-125°C)
Curvature-Compensated BGR using TC of resistors [39]	0.6-μm CMOS	2 V	1.14 V	5.3 (0°C-100°C)
Curvature-Compensated BGR using nonlinear current [33]	2-μm CMOS	1.1 V	0.595 V	20 (-15°C-90°C)
CMOS Voltage Reference using DTMOS devices [40]	0.35-μm CMOS	0.85 V	0.650 V	57 (-50°C-75°C)
CMOS Voltage Reference using V_{TH} subtraction [44]	SOI-MOS	-	2.38 V	33.8 (-50°C-75°C)
CMOS Voltage Reference using V_{GS} subtraction [46]	0.6-μm CMOS	1.4 V	0.313 V	36.9 (0°C-100°C)
CMOS Voltage Reference using ZTC point[14]	0.35-μm CMOS	3.3 V	0.799 V	13 (-20°C-100°C)
CMOS Voltage Reference presented in Section 5.1	0.18-μm CMOS	1.8 V	0.703 V	28 (-50°C-150°C)
CMOS Voltage Reference presented in Section 5.3	0.18-μm CMOS	1.8 V	0.640 V	4 (-50°C-150°C)
CMOS Voltage Reference presented in Section 5.4	0.18-μm CMOS	1.8 V	0.640 V	4 (-50°C-150°C)

5.6 Conclusion

In this chapter, three new voltage reference circuits were proposed and designed in 0.18-μm technology. First, a voltage reference was presented which takes advantage of summing the gate-source voltages of two diode-connected transistors biased by temperature-stable currents. The temperature coefficient of the output voltage of this reference was shown to be 28 ppm/°C over the temperature range of -50°C to 150°C. It was also shown that the temperature dependence of the gate-source voltage of a CMOS transistor biased with a PTAT current source can be controlled by the parameters of the PTAT current source. Based on this idea, two voltage references were designed and implemented in 0.18-μm technology. The temperature dependence of the reference voltage in both circuits was found to be 4 ppm/°C over the range of -50°C to 150°C. Finally, the performance of the proposed voltage references was compared with other voltage references in the literature and it was concluded that our voltage references have a performance comparable with the bandgap voltage references and a better performance than the non-bandgap ones.

Chapter 6

Conclusion

Current and voltage references find applications in a variety of analog and digital circuits and systems. Designing a reference merits the scrutiny of several factors. Temperature-drift is one of the most important issues with which to contend.

The temperature drift of the current references must be well characterized and controlled. There are four types of current references used in circuit designs. The most frequently used current reference is a PTAT current reference which generates a current which is linearly proportional to temperature. A CTAT current, the complement of PTAT, is also used as a reference current. Temperature-independent current references are usually designed based on properly combining temperature-dependent currents or using available voltage references. Finally, a $PTAT^2$ reference is another useful type of a current reference which generates a current that is proportional to the square of the temperature.

Voltage references are divided into three categories when considering temperature compensation. A zero-order reference simply is a naturally existing voltage (such as a Zener diode) that does not fluctuate significantly with operating conditions. There is no effort on the part of the designer to improve the existing tolerance of the given

voltage. When the accuracy is improved by attempting to cancel the first-order term of the polynomial relationship with respect to temperature, the order of the reference is increased by 1. Finally, curvature-corrected references improve the accuracy by cancelling the second-order and higher-order components of the given voltage. The most widely used first-order or higher-order voltage reference is a bandgap reference. Its output voltage is referred to the bandgap energy of silicon and is stable against temperature and process variations. Bandgap references are bipolar in nature but can also be implemented in any standard CMOS technology, using parasitic vertical BJTs. As an alternative, voltage references in MOS technology can also be implemented using the threshold voltage difference. However, this technique is not applicable in standard low-cost CMOS technologies since additional fabrication steps are needed. Exploiting the presence of the ZTC point has also been proposed and used for the design of CMOS voltage references, but this technique might not be suitable for low voltage design. In this thesis, the techniques used for the design of these references, as well as the advantages and disadvantages of each method were studied.

The main contributions of this thesis are highlighted below.

1. A new CMOS voltage reference using two diode-connected NMOS transistors biased by constant currents has been designed and implemented in 0.18-μm technology. The circuit was designed using gate-source voltage summation of two NMOS transistors, which show opposite temperature behaviors. The temperature coefficient of the output voltage of this reference has been found to be 28 ppm/°C over the temperature range of -50°C to 150°C.

2. The temperature behavior of the gate-source voltage of a CMOS transistor biased by a PTAT current source has been investigated analytically. It was shown that

the temperature-coefficient of the gate-source voltage of the transistor can be controlled by the parameters of the PTAT current source. This idea can be used for the design of CMOS voltage reference.

3. A new CMOS voltage reference consisting of a PTAT current source and a diode-connected NMOS transistor has been proposed and realized in 0.18-μm technology. The parameters of the PTAT current source have been chosen so that the gate-source voltage of the diode-connected transistor shows minimum temperature dependence. Simulation results have shown a temperature coefficient of 4 ppm/°C over the range of -50°C to 150°C.

4. A new CMOS voltage reference, which takes advantage of summing the gate-source voltages of two diode-connected transistors biased by PTAT currents, has been implemented in 0.18-μm technology. The diode-connected transistors have been biased below their ZTC points and, therefore, this circuit is able to operate with sub-1-V power supply. The circuit has been simulated over the temperature range of -50°C to 150°C and the reference voltage shows a temperature coefficient of 4 ppm/°C.

5. The performances of the proposed voltage references were compared with other voltage references in the literature and it was shown that our voltage references have a performance comparable with the bandgap voltage references and a better performance than the non-bandgap ones.

References

[1] G. A. Rincon-Mora, *Voltage References, From diodes to precision high-order bandgap circuits.* NJ, U.S.A.: IEEE Press and Wiley Interscience, 2002.

[2] C. Toumazou, G. Moschytz, and B. Gilbert, *Trade-Offs in Analog Circuit Design, The Designer's Companion.* Kluwer Academic Publisher, 2002.

[3] B. Song and P. Gray, "A precision curvature-compensated CMOS bandgap reference," *IEEE Journal of Solid-State Circuits*, vol. 18, no. 6, pp. 634–643, Dec. 1983.

[4] K. Leung and P. Mok, "A sub-1-V 15-ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 4, pp. 526–530, Apr. 2002.

[5] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, May 1999.

[6] R. A. Blauschild, P. A. Tucci, R. S. Muller, and R. G. Meyer, "A new NMOS temperature-stable voltage reference," *IEEE Journal of Solid-State Circuits*, vol. 13, no. 6, pp. 767–774, Dec. 1978.

[7] J. C. Harvey, "Techniques for a high temperature CMOS operational amplifier," M.S. thesis, Case Western Reservce University, Jan. 1998.

[8] D. L. Pulfrey and N. G. Tarr, *Intoduction to Microelectronic Devices.* New Jersey: Prentice Hall, 1989.

[9] S. M. Sze, *Physics of Semiconductor Devices.* New Jersey: John Wiley and Sons, 1981.

[10] S. M. Sze, *Semiconductor Devices, Physics and Technology*, 2nd ed. New York: John Wiley and Sons, 2002.

[11] F. M. Klaassen and W. Hes, "On the temperature coefficient of the MOSFET threshold voltage," *Solid State Electron*, vol. 29, no. 8, pp. 787–789, 1986.

[12] Z. D. Prijic, "Analysis of temperature dependence of CMOS transistors' threshold voltage," *Microelectronic Reliable*, vol. 31, no. 1, pp. 33–37, 1991.

[13] Y. P. Tsividis, *Operational and Modeling of the MOS Transistor.* New York: McGraw-Hill, 1987.

[14] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *IEEE Transactions on Circuits and Systems-I*, vol. 48, no. 7, pp. 876–883, July 2001.

[15] K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems.* New York: McGraw-Hill, 1994.

[16] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed. New York: John Wiley and Sons, 2001.

[17] F. Maloberti, *Analog Design for CMOS VLSI Systems*. The Netherlands: Kluwer Academic Publishers, 2001.

[18] W. T. Harrison, J. A. Connelly, and R. Stair, "An improved current-mode CMOS voltage refrence," in *Proc. Southwest Symposium on Mixed-Signal Design*, Feb. 2001, pp. 23–27.

[19] R. Stair, J. A. Connelly, and M. Pulkin, "A current-mode CMOS voltage refrence," in *Proc. Southwest Symposium on Mixed-Signal Design*, Feb. 2000, pp. 23–26.

[20] D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: John Wiley and Sons, 1997.

[21] I. M. Filanovsky, "An input-free V_T extractor circuit using a series connection of three transistors," *Int. J. Electronics*, vol. 82, no. 5, pp. 527–532, 1997.

[22] P. Malcovati, F. Maloberti, M. Pruzzi, and C. Fiocchi, "Curvature compensated BiCMOS bandgap with 1 V supply voltage," in *Proc. IEEE European Solid-State Circuits Conference (ESSCIRC '00)*, 2000, pp. 52–55.

[23] M. Martins and J. Dias, "CMOS shunt regulator with bandgap reference for automotive environment," *IEE Proceeding Circuits Devices and Systems*, vol. 141, pp. 157–161, June 1994.

[24] H. Tanaka, "Sub 1-μA dynamic reference voltage generator for battery operated DRAMs," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 4, pp. 448–453, Apr. 1994.

[25] D. Hilbiber, "A new semiconductor voltage standard," *ISSCC Digest Technical Papers*, vol. 7, pp. 32–33, 1964.

[26] R. Widlar, "Some circuit design techniques for linear integrated circuits," *IEEE Transactions on Circuits and Systems*, vol. 12, no. 4, pp. 586–590, Dec. 1965.

[27] R. Widlar, "New developments in IC voltage regulators," *IEEE Journal of Solid-State Circuits*, vol. 6, no. 1, pp. 2–7, Feb. 1971.

[28] K. Kuijk, "A precision reference voltage source," *IEEE Journal of Solid-State Circuits*, vol. 8, no. 3, pp. 222–226, June 1973.

[29] A. Brokaw, "A simple three-terminal IC bandgap reference," *IEEE Journal of Solid-State Circuits*, vol. 9, no. 6, pp. 388–393, Dec. 1974.

[30] G. Meijer and J. Verhoeff, "An integrated bandgap reference," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 403–406, June 1976.

[31] R. J. Widlar, "Low voltage techniques," *IEEE Journal of Solid-State Circuits*, vol. 13, pp. 838–846, Dec. 1978.

[32] I. Lee, G. Kim, and W. Kim, "Exponential curvature-compensated BiCMOS bandgap reference," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 11, pp. 1396–1403, Nov. 1994.

[33] G. Rincon-Mora and P. Allen, "A 1.1 V current-mode and piecewise-linear curvature corrected bandgap reference," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1551–1554, Oct. 1998.

[34] S. Lewsi and A. Brokaw, "Curvature correction of bipolar bandgap references," U.S patent 4 808 908, Feb. 1989.

[35] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE Journal of Solid-State Circuits*, vol. 12, no. 6, pp. 224–231, June 1977.

[36] Y. Tsividis, "Accurate analysis of temperature effects in I_C-V_{BE} characteristics with application to bandgap reference sources," *IEEE Journal of Solid-State Circuits*, vol. 15, no. 6, pp. 1076–1084, Dec. 1980.

[37] A. Boni, "Op-Amps and startup circuits for CMOS bandgap references with near 1-V supply," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 10, pp. 1339–1343, Oct. 2002.

[38] Y. Jiang and E. K. Lee, "Design of low-volatge bandgap reference using transimpedance amplifier," *IEEE Transactions on Circuits and Systems-II*, vol. II, pp. 552–555, June 2000.

[39] K. Leung, P. Mok, and C. Leung, "A 2-V 23μA 5.3-ppm/°C Curvature-Compensated CMOS Bandgap Voltage Reference," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 561–564, Mar. 2003.

[40] A. Annema, "Low-power bandgap references featuring DTMOST's," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 7, pp. 949–955, July 1999.

[41] http://public.itrs.net/, "The ITRS Home page," .

[42] H. Neuteboom, B. J. Kup, and M. Janssens, "A DSP-based hearing instrument IC," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 1790–1806, Nov. 1997.

[43] M. Ugajin, K. Suzuki, and T. Tsukaraha, "A 0.6-V supply, voltage-reference circuit based on threshold-voltage-summation architecture in fully-depleted

CMOS/SOI," *IEICE Transactions on Electronics*, vol. E85-C, no. 8, pp. 1588–1595, August 2002.

[44] H. J. Song and C. Kim, "A temperature-stabilized SOI voltage reference based on threshold voltage difference between enhancemenr and depletion NMOSFET's," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 6, pp. 671–677, June 1993.

[45] K. N. Leung and P. K. T. Mok, "A CMOS voltage reference based on weighted difference of gate-source voltages between PMOS and NMOS transistors for low dropout regulators," in *Proc. IEEE European Solid-State Circuits Conference (ESSCIRC '01)*, 2001, pp. 88–91.

[46] K. N. Leung and P. K. T. Mok, "A CMOS voltage reference based on weighted ΔV_{GS} for CMOS low-dropout linear regulator," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 1, pp. 146–150, Jan. 2003.

[47] T. Manku and Y. Wang, "Temperature-independent output voltage generated by threshold voltage of an NMOS transistor," *IEE Electronics Letters*, vol. 31, no. 12, pp. 935–936, June 1995.

[48] I. M. Filanovsky, "Voltage reference using mutual compensation of mobility and threshold voltage temperature effects," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS '00)*, 2000, pp. 197–200.

Vita

Laleh Najafizadeh

EDUCATION

September 2001 – October 2003

University of Alberta M.Sc. Electrical and Computer Engineering

September 1995 – June 1999

Isfahan University of Technology B.Sc. Electrical and Computer Engineering

WORK EXPERIENCE

Research Assistant, University of Alberta,

Department of Electrical and Computer Engineering, 2001-present

Teaching Assistant, University of Alberta,

Department of Electrical and Computer Engineering, 2001-present

Electronics Engineer, Isfahan Telecommunication Company,

Isfahan, Iran, 1999-2001

AWARDS

Delta Kappa Gamma World Fellowship (2003-2004)

Alberta Ingenuity Fund (2004)

PUBLICATIONS

I. M. Filanovsky, and L. Najafizadeh, "Zeroing in on a zero-temperature coefficient point," Proc. 45th *IEEE Midwest Symp. Circuits and Systems*, Vol. 1, pp.271-274, Tulsa, OK, August 2002.

L. Najafizadeh, and I. M. Filanovsky, "Towards a sub-1-V CMOS voltage reference", Submitted to *IEEE International Symposium on Circuits and Systems* 2004.

L. Najafizadeh, and I. M. Filanovsky, "A simple voltage reference using transistor with ZTC point and PTAT current source", Submitted to *IEEE International Symposium on Circuits and Systems* 2004.